Charging and Discharging Characteristics of Stacked Floating Gates of Silicon Quantum Dots

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1. Introduction

Implementation of silicon-quantum-dots (Si-QDs) as a floating gate in metal-oxide-semiconductor field-effect transistors (MOSFETs) has received increasing attention because of its potential advantage for multivalued memories operating reliably even at room temperature and above [1-3].

In this work, we focused on electron storage in Si-QDs stack structures and studied electron charging, discharging and retention characteristics of the stack structures as floating gate in MOS capacitors in comparison to those of a single Si-QDs floating gate.

2. Experimental

Hemispherical and single-crystalline Si-QDs were self-assembled on 2.8nm-thick SiO_2 layer by controlling the early stages of LPCVD of pure SiH_4 at 570°C under a pressure of 0.2 Torr[4,5]. The surface of the first Si-QDs layer was oxidized at 850°C in Dry O_2 to be uniformly covered with ~1nm-thick SiO_2. Double-stacked or triple-stacked structures consisting of Si-QDs and ~1nm-thick SiO_2 were also fabricated by repeating the formation of Si-QDs and their surface oxidation. The average dot height and the total dot density for each single Si-QDs layer evaluated by atomic force microscopy (AFM) were ~6.0nm and $1.6x10^{11}cm^{-2}$, respectively. To form a 7.5nm-thick control oxide conformally on the Si-QDs layer(s), a 3.3nm-thick amorphous Si layer was first grown over the 1nm-thich SiO_2 layer on dots by LPCVD of 10% Si_2H_6 diluted with He at 440°C, and fully oxidized in dry O_2 at 1000°C and Al gates were fabricated. Finally, the MOS capacitors were annealed in H_2 at 400°C.

3. Results and Discussion

The capacitance-voltage (C-V) curves of Si-QDs floating gate MOS capacitors show hysteresis characteristics being attributable to charging and discharging of Si-QDs floating gates as shown in Fig. 1. In contrast, no hysteresis was observable in the C-V curve of the MOS capacitor fabricated without the dot formation and the flat band voltage was quite reasonable. In each case with the Si-QDs floating gate, when the gate voltage was swept from +2V toward the negative bias side, the positive flat-band voltage shift were first measured until the capacitance peak appears around the flat-band condition and then ΔVfb became negative reflecting the hole injection presumably to the floating gate. As for positive ΔVfb measured firstly, the increase of ΔVfb becomes small with

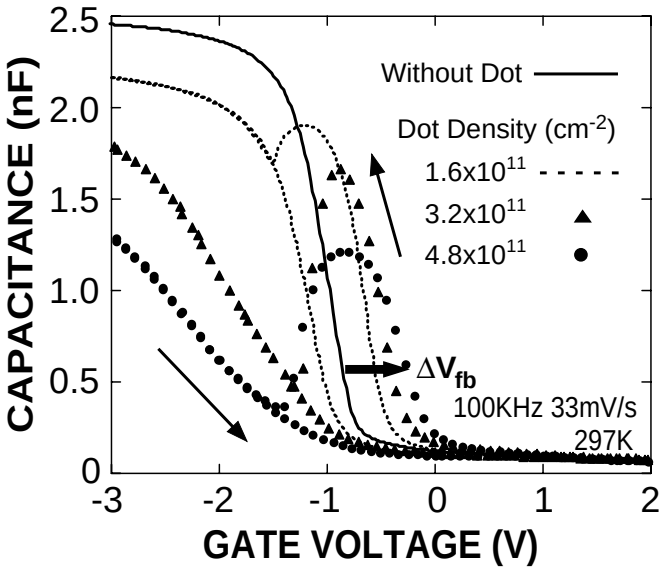

Fig. 1 Capacitance-voltage characteristics of Si-QDs floating gate MOS capacitors measured at room temperature and at 100kHz. The number of dots was changed in the range of $1.6\text{-}4.8x10^{11}cm^{-2}$ in areal density.

an increase of the number of dot stack, which suggests that the Coulomb interaction among the neighboring charged Si-QDs becomes significant with increasing total number of dots. From the observed reduction in the accumulation capacitance with increasing number of dot stack, each Si-QDs layer was estimated to be equivalent to 4nm-thick single Si layer, reasonably. Notice that, in the negative bias region beyond the flat-band condition, the slop becomes small with increasing number of dot stack although the C-V curves show no hysteresis. This indicates that numbers of holes can injection to the SiQDs floating gate but can not retain stably in the SiQDs floating gate, presumably because holes generated in the Si-QDs by the emission of valence electrons from the Si-QDs can smoothly recombine with electrons tunneling through the 2.8nm-thick bottom SiO_2 in sweeping the gate voltage toward the positive bias side.

Retention characteristics of charged and discharged states were evaluated after fully electron charged at +3V and discharged at -3V. Figure 2 shows the results for the case with the triple-stack Si-QDs floating gate. The temporal changes in flat-band voltage at +0.2 and +0.8V show that charged and discharged states are stably obtained after just a lapse of 500s, respectively, because of

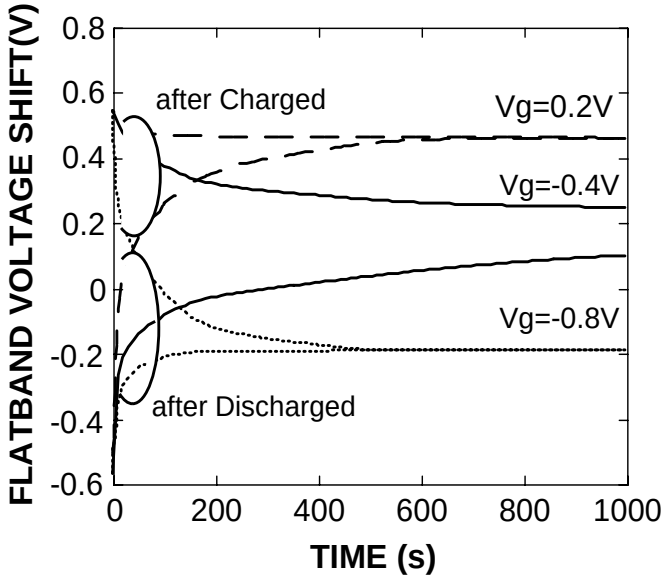

Fig. 2 Charge retention characteristics of the MOS capacitor with the triple-stack Si-QDs floating gate, where the temporal changes in the flat-band voltage were measured at +0.2, -0.4 and -0.8V after fully electron charged at +3V and discharged at -3V.

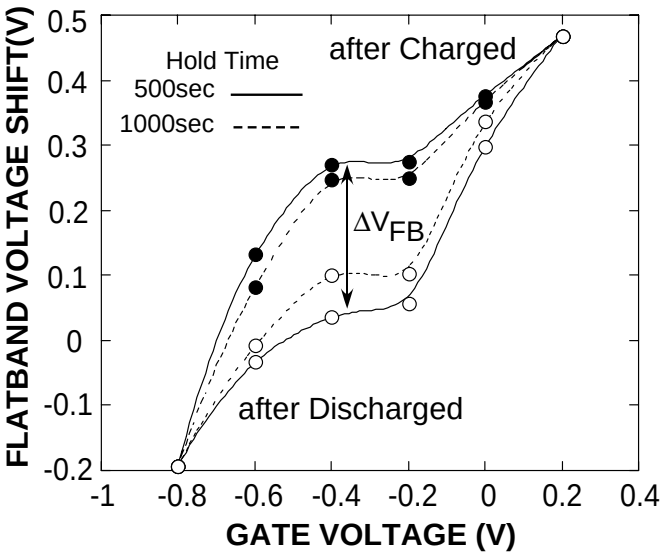

Fig. 3 Flat-band voltage shifts versus gate voltage for charged and discharged states after a lapse of 500 or 1000s as seen in Fig. 3.

the bottom tunnel oxide as thin as 2.8nm. When the gate voltage is set at -0.4V, two metastable states separated by ~0.2V in the flat-band voltage can be still observable after a lapse of 1000s.

Figure 3 summarize the flat-band voltage shifts after a lapse of 500 or 1000s since the triple-stack Si-QDs floating gate was fully charged or discharged as a function of the gate voltage. In the depletion region, especially in the range from -0.2 to -0.4V, a relatively long retention for both charged and discharged states was obtainable. To compare the retention characteristics of the single, double-stack and triple-stack Si-QDs floating gates, we defined ΔV_{FB} as the difference in the flat-band voltage shift between the two states as seen in the gate voltage range from -0.8 to 0.2V of Fig. 4 as ΔV_{FB} and plotted the ratio of ΔV_{FB} after a lapse of 1000s to initial value (ΔV_{FB0}) as a function of the gate voltage as indicated in Fig. 4. Obviously, the charge retention was improved by increasing number of dot stack, suggesting that the electron tunneling between different energy states among neighboring Si-QDs plays a role in progress of charging and discharging for the stacked dots floating gate.

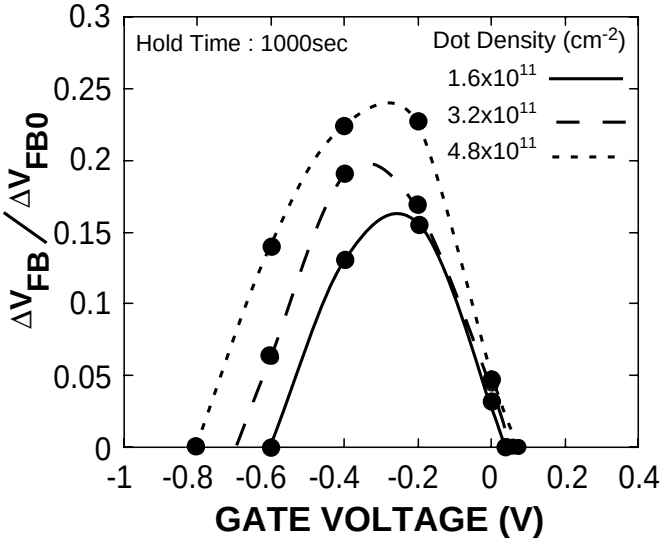

Fig. 4 Gate voltage dependence of the ratio of ΔV_{FB} after a lapse of 1000s to the initial value (ΔV_{FB0}) for each of the single, double-staked and triple-stack Si-QDs floating gates.

4. Conclusions

For MOS capacitors with the Si-QDs floating gates, the hole injection to Si-QDs was observed in the negative bias region beyond the flat-band condition accompanied with no C-V hysteresis and symmetric I-V characteristics. This suggests that holes generated in Si-QDs can smoothly recombine with electrons tunneling through the 2.8nm-thick bottom SiO_2. In addition, the retention characteristics are improved by the use of stacked Si-QDs floating gates in MOS capacitors. It is likely that the electron tunneling between different energy states among neighboring Si-QDs involves the improvement of retention characteristics.

Reference

[1] S. Tiwari, F. Rana, H. Hanafi, H. Hartstein, E. F. Crabbe and K. Chan, Appl. Phys. Lett. 68 (1996) 1377.

[2] S. Tiwari, F. Rana, K. Chan L.Shi and H. Hanafi, Appl. Phys. Lett. 69 (1996) 1232.

[3] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki and M. Hirose, Jpn. J. Appl. Phys. 40 (2001) L721.

[4] T. Shibaguchi, Y. Shimizu M. Ikeda H. Murakami and S. Miyazaki, Proc. of Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Device (2003) 151.

[5] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki, Jpn. J. Appl. Phys. 42 (2003) 4134.

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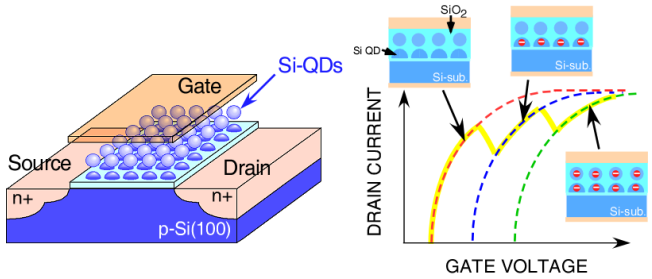
Background

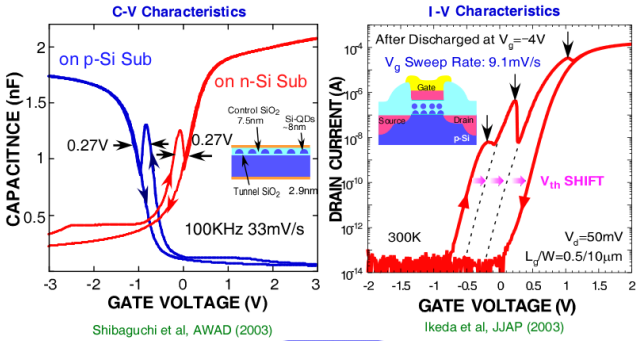


- Charging Energy
- Quantization Energy

➡

- Discrete Charged States of the Si-QDs Floating Gate
- Multivalued Operation at Room Temperature

Our Previous Work



Shibaguchi et al, AWAD (2003)

Ikeda et al, JJAP (2003)

This Work

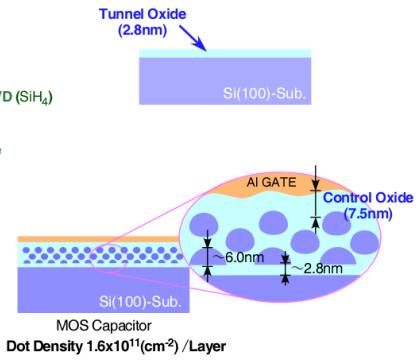
Stacked Si-QDs Floating Gate MOS Capacitors ➡

- Charging and Discharging Characteristics
- Retention Characteristics

Fabrication of Si-QDs Floating Gate MOS Capacitors

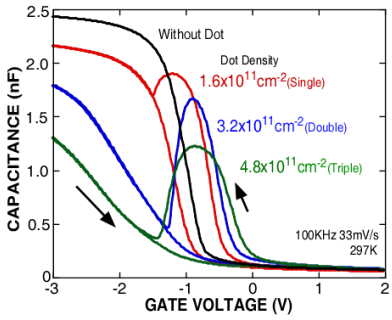
For MOS Capacitors
p-Si(100)(1x10^{15}cm^{-3})

- **Oxidation** 2%Dry O_2, 1000℃
- **0.1% HF Treatment**
- **Si-QDs Fabrication by LPCVD (SiH_4)** 570℃, 0.2Torr, 1min
- **Oxidation of Si-QDs Surface** 2%Dry O_2, 850℃
- **a-Si Deposition & Oxidation**
  a-Si Deposition (3.3nm)
  Si_2H_6: 440℃, 0.2Torr
  a-Si Oxidation
  2%Dry O_2, 1000℃
- **Gate Fabrication** Al Gate 1mmϕ
- **H_2 Anneal** 400℃ 30min



MOS Capacitor
Dot Density 1.6x10^{11}(cm^{-2}) /Layer

C-V Characteristics of Floating Gate MOS capacitors with and without Si-QDs



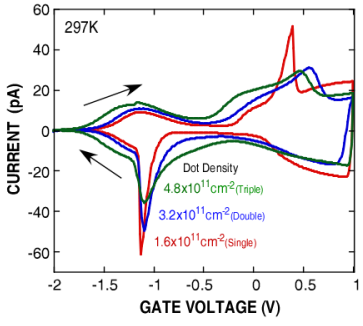
	Positive ΔV_{FB} by electron injection
Single	0.32V
Double	0.49V
Triple	0.65V

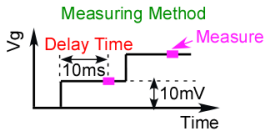
Negative ΔV_{FB} but no hysteresis

➡ Hole injection Si-QDs floating gate

★ Smooth recombination with electrons tunneling through the bottom oxide

Transient Current-Voltage Characteristics of Si-QDs Floating Gate MOS Capacitors





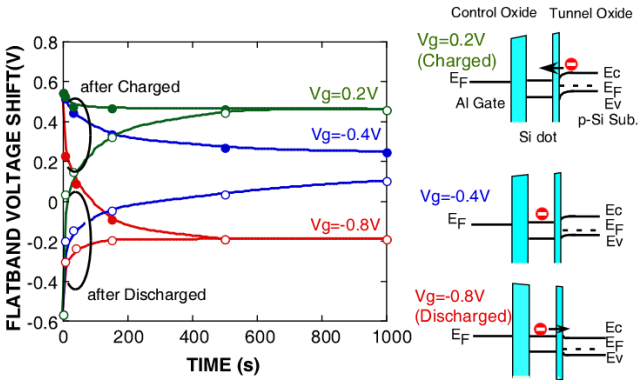
★Negative current peaks at ~-1.1V

➡ Emission of remaining electrons from Si-QDs floating gate

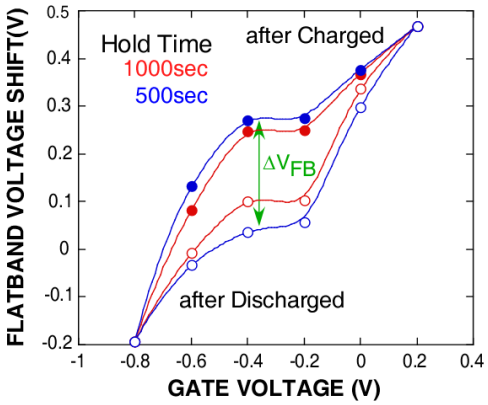
★Broad negative current peaks for the stack structure

➡ The slow emission rate of electrons stored in the Si-QD layer far from the substrate.

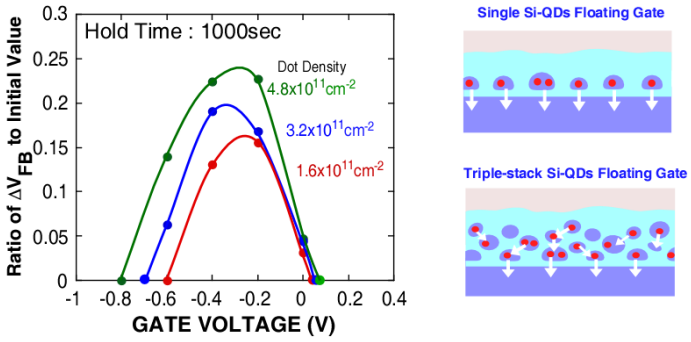
Charge Retention Characteristics of the MOS Capacitor with the Triple-stack Si-QDs Floating Gate



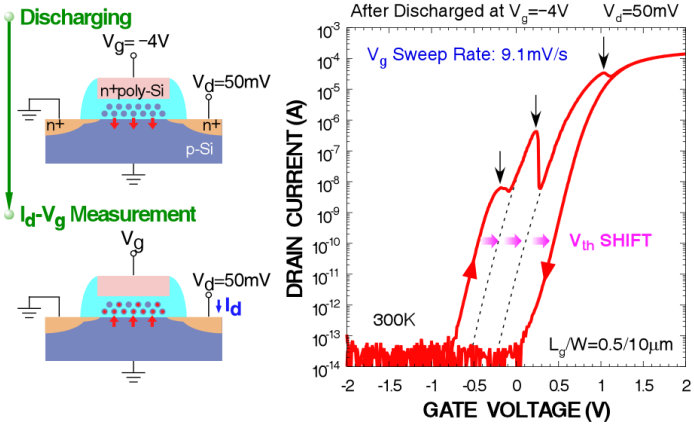
Flat-band Voltage Shifts versus Gate Voltage for Charged and Discharged States



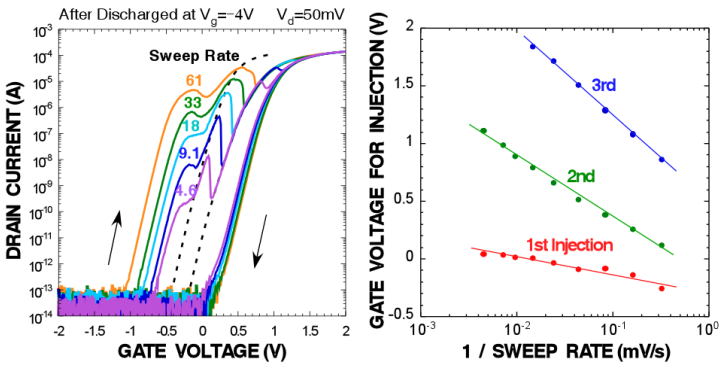
Gate Voltage Dependence of the Ratio of ΔV_{FB} after a Lapse of 1000s to the Initial Value



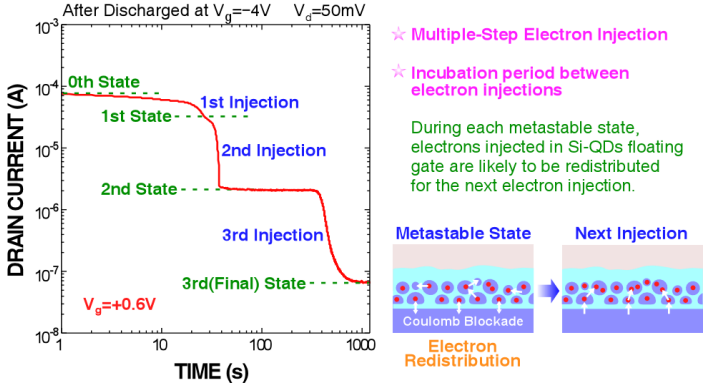
I_d-V_g Characteristics for MOSFET with Doubly-Stacked Si-QDs Floating Gate



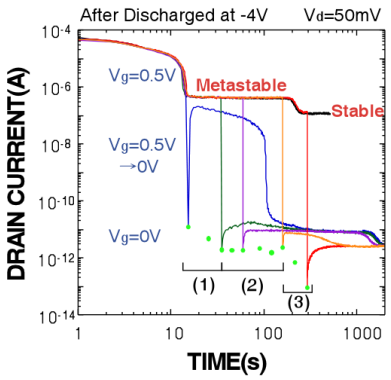
Sweep Rate Dependence of I_d-V_g Characteristics

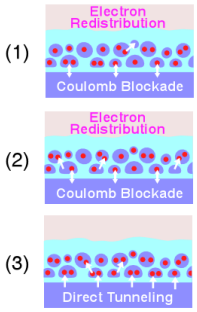


Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate



Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate





Average dot height: 6nm
Mean distance between dots for the 1st dot layer: 17nm

Summary

MOS capacitors with the Si-QDs floating gates

- As for the positive flat band voltage shift, an increment of ΔVfb becomes small with an increase of the number of dot stack.
  - ➡ Coulomb interaction among the neighboring charged Si-QDs become significant with increasing total number of dots.
- The hole injection to Si-QDs was observed no C-V hysteresis and symmetric I-V characteristics.
  - ➡ Holes generated in Si-QDs can smoothly recombine with electrons tunneling through the bottom SiO_2.
- The retention characteristics are improved by stacking Si-QDs.
  - ➡ Electron tunneling between different energy states among neighboring Si-QDs involves the improvement of retention characteristics.

n-MOSFETs with Si-QDs Floating Gate

- Room Temperature Memory Operation
  - Multistep Electron Charging

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This work has been supported in part by a Grant-in-Aid for the 21st Century COE program from the Ministry of Education, Science, Sports and Culture of Japan.