A 3D Integration Architecture utilizing Wireless Interconnections for Implementing Hyper Brains

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1. Research Target

Recently, in order to break Moore's law, 3-dimensional (3D) integration technologies are extensively studied for increase a scale of integration and processing capability.

(Fig.1) Inter connection technologies using via-holes and micro bumps have been developed, but fabrication cost and yield problems are still unresolved. To overcome these problems, wireless capacitive coupling, wireless inductive coupling [1] and optical interconnection were proposed. These techniques are competitive, but will be applied to 3D integration in combined schemes, because each has a suitable range of communication (Fig. 2).

2. 3D integration Architecture

From the view point of a complete system, global interconnects throughout whole chips and local parallel interconnects between adjacent chips are required. The former is used for system clocking as well as busses which enables synchronous processing accessing to a G-byte database. The latter transfers 2D data such as image data, without the requirement of gathering and multiplexing.

The proposed local wireless interconnection scheme (LWI) between chips utilizes the principle of magnetic coupling and resonation of on-chip spiral inductors. A circuit schematic and an inductor structure are shown in Fig. 3.

The test chips were developed with 0.25μm and 0.18μm CMOS technologies. Two chips were mounted on manipulators for measuring the transfer characteristics. A data rate of 1Gbps was obtained with 1mW power dissipation.[2] The LWI can be applied to asynchronous interconnects corresponding to wires as well as synchronous systems. By optimizing inductor size, chip thickness and power dissipation, it is possible to transfer data in highly parallel form between neighboring chips.

3. Multi-chip Vision processing with PWM signaling and LWI

A multi-chip vision (MCV) system based on hierarchical biological processing has been investigated. A MCV test chip which consists of a pixel array and a PWM-based line parallel I/O was developed with a 0.35μm CMOS technology. Two MCV chips are connected with two LWI chips using analog PWM signaling as shown in Fig. 3. Pixel output voltage of MCV1 is modulated to an analog PWM signal. It is re-modulated to the RZ signal and drives the TX MOST. The received signal is detected by a comparator and reconstructed to the original PWM signal. P_{1o} and P_{2i} are the PWM output of MCV1 and the PWM input to MCV2, respectively. $v_o(1)$ and $v_o(2)$ are output voltages, without smoothing and with smoothing, respectively.

The global wireless interconnection (GWI) utilizes electro-magnetic (EM) wave transmission using integrated antennas were proposed by Prof. Kikkawa's group. A 20GHz sinusoidal wave propagates with a low loss of 0.14dB/chip. Clock distribution at over 10GHz could be implemented with a sinusoidal wave transmission.

3D integration using GWI and LWI, called 3-dimensional custom stack system (*3DCSS*), is proposed.[3] By the *3DCSS* concept, over 10 chips can be stacked as shown in Fig. 4. Required alignment accuracy of chips is very relaxed and as low as about half of the inductor size. Power/Ground pins are bonded with existing techniques. The feature of *3DCSS* is to realize a flexible customized system integrating various kinds of chips with a wireless interface. Yield and Known Good Die problems are also resolved by chip testing using wireless test head.

4. Hyper Brain Architecture

For implementing a hyper brain, the concept of a multi-object recognition system using the *3DCSS* concept has been studied. We have adopted the Principal Component Analysis and the Eigen Face method for realizing multi-object detection and recognition in a natural scene. The proposed hyper brain is composed of wireless interconnected multiple chips including image sensor, early vision processor, object detector, feature detector, object recognizer and database, as shown in Fig. 5. The expected performance is 10 frame/s frame rate, 10 objects and 1000 data/object matching.

For implementing 3D hyper brain, the object detection with stereoscopic image processing, the modular learning model for robot brain, the low voltage loe noise analog processing, 10GHz clocking and wireless techniques have been also studied

References [1] D.Mizoguchi et al. A 1.2Gb/s/pin Wireless Superconnect based on Inductive Inter-Chip Signaling (IIS), ISSCC Digest of Tech. Papers, pp142-143, 2004.
[2] M. Sasaki and A. Iwata, A 0.95mW/1.0Gbps Spiral Inductor Based Wireless Chip-Interconnection with Asynchronous Communication Scheme, Symposium on VLSI Circuits, 22-3, 2005.
[3] A. Iwata, M. et. al., A 3D Integration Scheme Utilizing Wireless Interconnections for Implementing Hyper Brains, ISSCC2005 Dig. of Tech. Papers, pp.262-263, 2005.

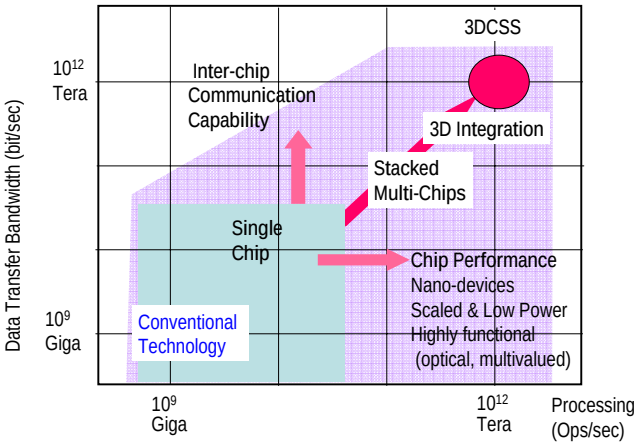


Fig. 1 Terabit Information Processing System

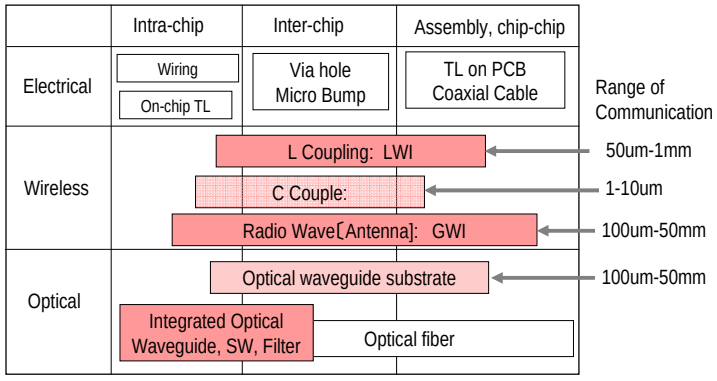
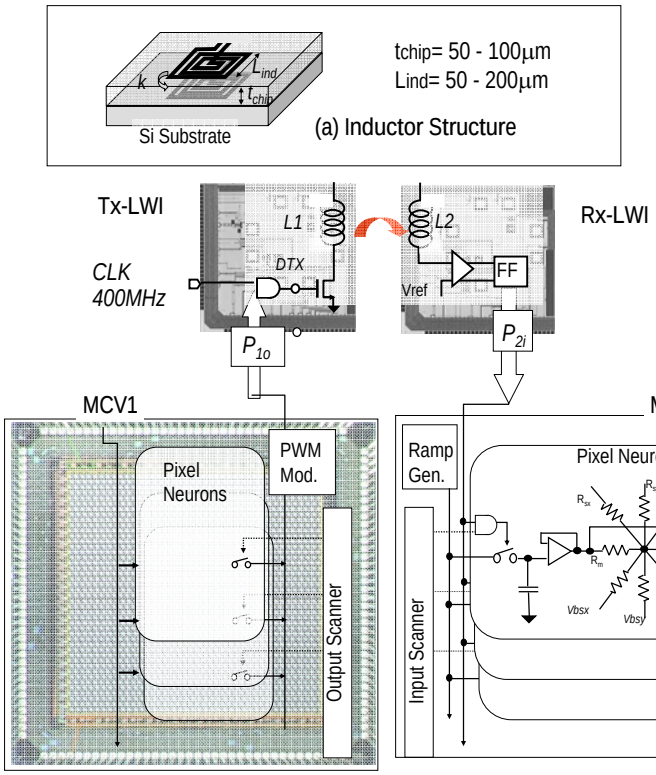
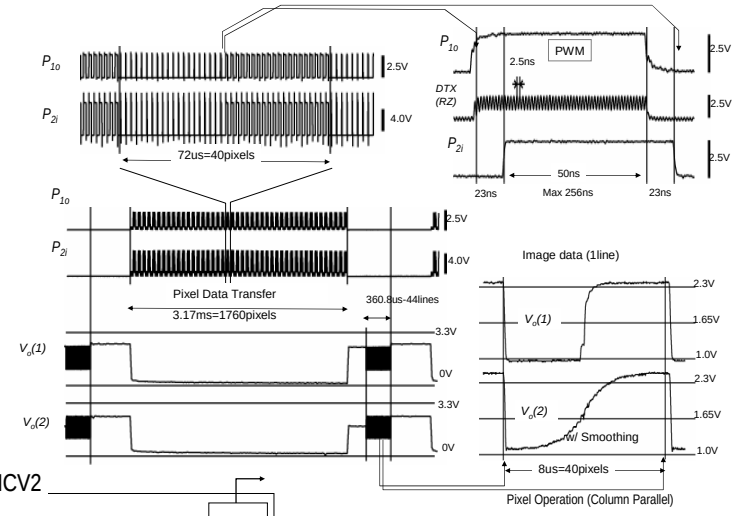


Fig. 2 Various Interconnection Techniques for Advanced Integration Systems





Measured Waveforms of MCV using Analog-LWI

Features of MCV Architecture
based on vertebrate visual systems
1. Time difference by analog memories
2. Space filtering by resistive networks
3. PWM-based line parallel I/O interface

Fig.3 Measurements of Multi-Chip Vision with LWI

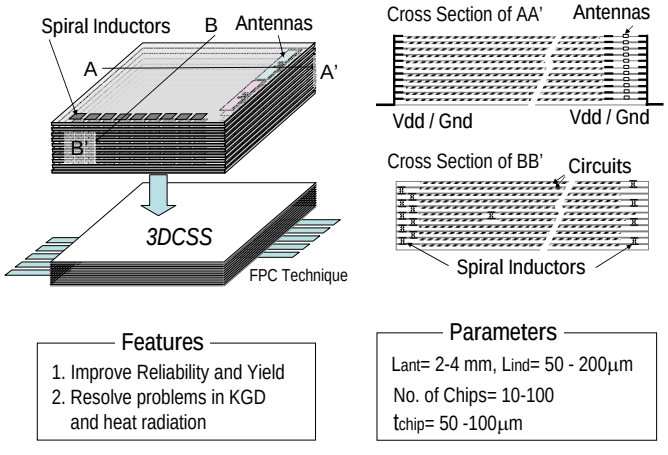


Fig.4 3DCSS Structure

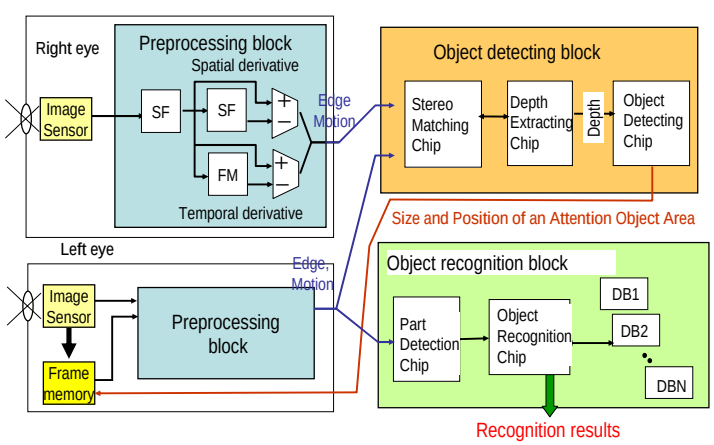
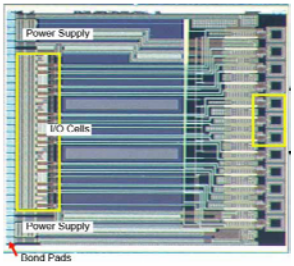


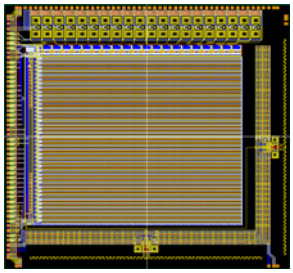
Fig.5 Hyper Brain Architecture with Multi-Object Recognition Capability

Members and Research Subjects

[Group Leader] Atsushi Iwata, [Sub Leader] Mamoru Sasaki
[3DCSS wireless Interconnection and Vision and Recognition System]

Joint Research Group
Poster number





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Daisuke Arizono (M2)
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Multi-chip Vision
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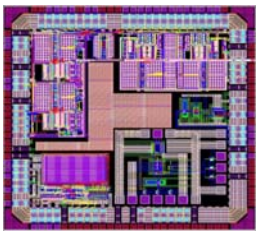
Hiroshi Ando ⟷ Mattaush Group
Multi-Object recognition Algorithm and chip design

Kan'ya Sasaki
Object Detection by Stereo Visions

Masahiro Ono
Learning algorithm for Robot brain

[Low Voltage Analog Circuits]



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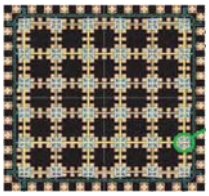
& Circuit design using HiSIM

[Ultra-high Frequency Circuits]



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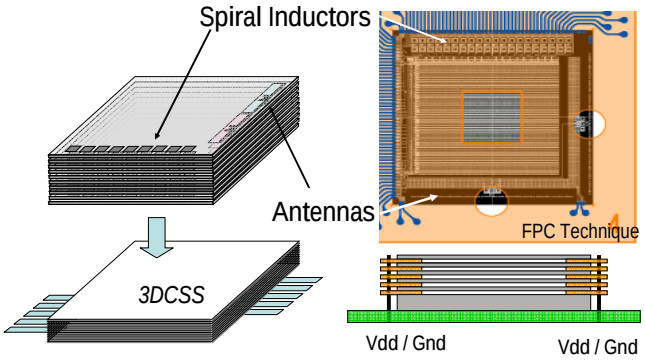
20GHz clock generation

Toru Mukai
20-30GHz RF Front-end

3D integration Structure



Features
1. Improve Reliability and Yield
2. Resolve problems in KGD and heat radiation

Parameters
L_{ant}= 2-4 mm, L_{ind}= 50 - 200μm
No. of Chips= 10-100
t_{chip}= 50 -100μm