Image-Scan Video Segmentation Architecture Based on Embedded Memory Technology

Takashi Morimoto, Hidekazu Adachi, Kosuke Yamaoka, Tetsushi Koide, and Hans Jürgen Mattausch

Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, Japan
Phone: +81-82-424-6265 Fax: +81-82-424-3499 e-mail: morimoto@rcns.hiroshima-u.ac.jp

Abstract

This paper presents an image-scan video segmentation architecture and its FPGA implementation. The proposed architecture uses high access-bandwidth embedded memories for storing all intermediate segmentation results of the complete image and an image-scan approach for segmentation processing with a small number of the processing elements. Since the proposed architecture becomes very compact, it promises the possibility of hardware implementation with an FPGA. We have verified that a real-time image segmentation prototype system for 80×60 pixels can be constructed with about a half logic elements of a standard FPGA device in 130nm CMOS technology.

1. Introduction

Recently, many methods for object-based visual information processing such as object-oriented image compression [1], object recognition or object tracking [2] have been proposed. These methods can be applied for robot-vision, intelligent transport systems [3], or the MPEG-7 standard [4]. In all of these methods, image segmentation is an indispensable first-step for object extraction.

Many image segmentation algorithms have already been proposed [5, 6]. However, the majority of these algorithms is implemented in software, and has large complexity so that hardware implementation is difficult. Recently, efficient real-time segmentation LSIs with pixel-based fully-parallel processing have been reported [7]. They are based on a network of processing elements, whose size is proportional to the number of pixels, so that application to large size images involves large hardware cost. Recently, technology development has enabled the integration of embedded memories with large storage capacity and large access bandwidth in FPGAs [8,9]. Therefore, exploitation of the large memory-access bandwidth for off-loading the intermediate segmentation status from the cell-network and image-scan-based processing with a small-size network of processing elements becomes realistic.

In this paper, we propose such a region-growing video segmentation architecture which exploits large access-bandwidth embedded memories for reducing the number of processing elements.

2. Image-Scan Video-Segmentation Architecture

The digital region-growing image segmentation algorithm which we proposed at the 2nd COE workshop can be realized by a fully-pixel-parallel cell-network-based architecture [7]. This architecture is suitable for high-end applications which require very short segmentation times. On the other hand, for cost-performance applications, in which the real-time processing is not necessary, we can reduce the implementation area consumption by relaxing the timing constraint.

The proposed implementation architecture reduces hardware cost by an image-scan approach. Figure 1 shows a conceptual diagram. The input image (*e.g.* 6×10 pixels) is divided into small pixel blocks (*e.g.* 6×2 pixels) from top to bottom. The pixels in each block are processed in parallel with a small image-segmentation processing array of the block size in sequential scan mode from top to bottom of the image. Between the processing steps of two blocks the processing results of the finished block are stored in an on-chip status memory and the processing status of next block, obtained in the previous scan of the image, is loaded into the processing elements of the array. These storing and loading steps require a memory with very high access bandwidth. Naturally, the block size is variable, and a trade-off can be exploited to optimize processing time versus hardware amount.

The image-scan approach is implemented with an architecture consisting of an embedded memory part and a processing part as shown in the block diagram of Fig. 2. The processing-part is further subdivided into weight calculation circuit and image segmentation block. The weight calculation block calculates the connection-weights from the pixel data (*e.g.* RGB values) of the input image, which stand for the similarity between neighboring pixels. The image segmentation block is a *m*×2 array of image segmentation elements (ISE), each corresponding to a processing element for one pixel. The image segmentation block executes the scan-mode region-growing by sequential processing of the image blocks. For this purpose the previous cell states and the connection weights are first loaded from the memory and after processing the new cell states are stored again for the block processing during the next scan. Loading and storing operations interact with the memory part. In the image segmentation block, a seed pixel for region-growing is selected, then region-growing

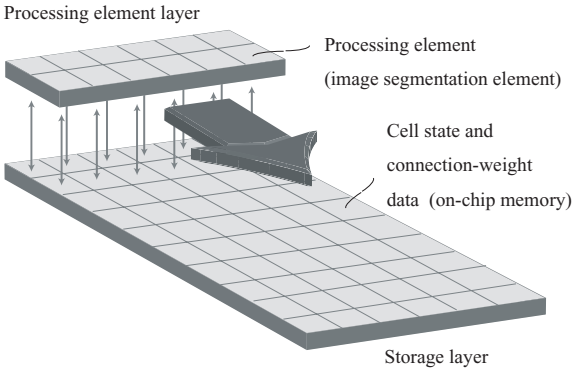

Fig.1 Conceptual diagram of image-scan video segmentation. High access-bandwidth is needed between the processing element layer and storage layer for real-time image processing. In this example, 6×2 processing elements are used for segmentation of a 6×10 pixel image.

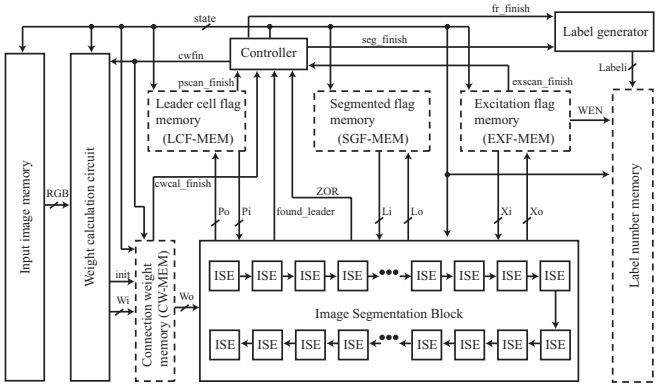

Fig.2 Block diagram of the row-scan based image segmentation architecture. The processing part is indicated by full-line boxes and the memory part is indicated by dashed-line boxes.

from this seed pixel is carried out with the ISE-array in parallel. When after several scans the current region cannot grown anymore, this region is defined as one segment and a label number is assigned to all of its pixels. Then the next seed pixel is search and used for a new region-growing process. In the described way, all pixels are classified into meaningful regions.

In the memory-part there are five kinds of memories, which are called excitation flag, segmented flag, leader cell flag, connection-weight and label number memory, respectively. The first 3 memories store the intermediate cell states during the region-growing processes and together with the connection-weight memory are connected to image segmentation block as shown in Fig. 2. The excitation flag memory (EXF-MEM) stores the corresponding cell's excitation states (X : 1bit, 0 or 1). The segmented flag memory (SGF-MEM) stores the indication whether the cells belong already to a segment or not (L : 1bit, 0 or 1). The region-growing seed or leader cell status of each cell is stored in the leader cell flag memory (LCF-MEM) (P : 1bit, 0 or 1). The connection weight memory (CW-MEM) is constructed with a bank structure, and each bank holds the corresponding connection-weights in such a way that all connection-weights of a block can be read in parallel. All status and connection-weight data for segmentation processing of $m\times2$ pixels are stored under the same address in each memory, so that they can be accessed simultaneously in one clock cycle.

3. FPGA-Based Video Segmentation System

For the verification of the proposed architecture, we are constructing an FPGA-based real-time image-segmentation prototype system (see Fig. 3) with a video-camera and a display. The segmentation quality and problems of the proposed architecture can be found by using this system more quickly and the visual inspection is more practical than circuit simulations.

A VGA-sized input image is resized to 80×60 pixels in the image resize block and stored in a clock-asynchronous external memory. Three external memories are used for holding 3 frames. This enables pipelining of the functions of transferring segmentation output to display, processing in the image segmentation block, and image input from the video-camera. The functionality of each memory is changed from input frame memory, processed frame memory to segmentation result output memory by the active frame selector in a cyclic way. Finally, pixel number and label data of each pixel are transferred to the image restore block for image resizing to the VGA via the labeled pixel extractor block. We can chose the display of any segmented region with the system's push-button switches. The specification of the segmentation system is summarized in Table I. Since the system is still under development, the exact usage of the FPGA-resources is not yet fixed. From the estimation, the usage of logic elements and on-chip internal memory will be about 50% and 2%, respectively.

With the latest generation of FPGA devices (*e.g.* Stratix II, EP2S180 [9]), QVGA-sized real-time (<33msec/frame) image segmentation can be achieved by the proposed approach. About 78000 adaptive look up tables (ALUTs) and 1.18Mbit memory are needed for the segmentation of QVGA images with a 320×2 sized ISE array. On the other hand, Stratix II (EP2S180) has a capacity of 143520 ALUTs and 9.38Mbit embedded memory. This corresponds to the 19% memory and 54% ALUTs usage of the Stratix II (EP2S180) FPGA chip. Consequently, single FPGA-chip real-time QVGA image segmentation becomes possible with the architecture proposed in this report.

Table I Specification of the developed image segmentation prototype system.

Input/output format	NTSC Y/C signal
Number of pixels (image segmentation)	4,800 pixels (80x60 pixels)
Number of image segmentation elements	160 ISE (80x2 ISE)
Clock frequency	12.27MHz
FPGA devices	Altera EP1S60F1020C7 Altera EPF10K250AGC599-3 Altera EPF10K40RC208-4
Code name	Magenta

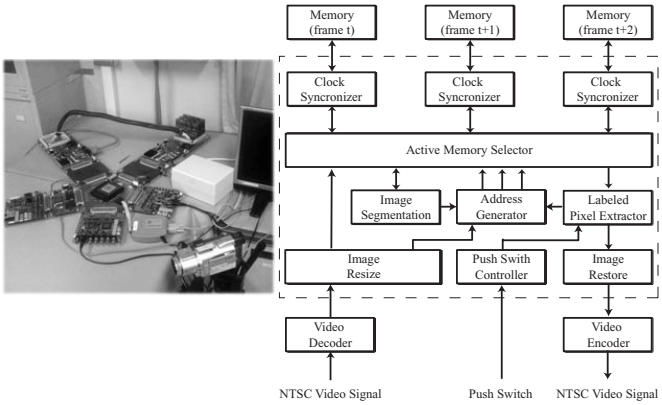

Fig.3 Left picture shows our video segmentation prototype system. The block diagram of this segmentation evaluation system is shown in the right figure.

5. Conclusion

A video segmentation architecture based on high bandwidth embedded memory and an image scan approach has been proposed. This architecture realizes real-time image segmentation with a compact processing circuit, whose size can be optimized in a trade-off with the processing time. An FPGA implementation verifies that QVGA size video segmentation on a single FPGA-chip becomes possible. Consequently, the proposed architecture can be applied to large-scale image segmentation with compact hardware in real-time.

Acknowledgments

Part of this work was supported by a Grant-in-Aid for young Scientists (B) (No.16700184), Ministry of Education, Culture, Sports, Science and Technology, Japanese Government and a Grant-in-Aid for JSPS Fellows, 1650741, 2005.

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Introduction

Video Segmentation

Extracting meaningful regions from natural input video pictures (30frame/sec) for higher level image processing applications such as object-oriented image compression, object recognition, object tracking.

Research Objectives

- For high-end applications which require very short segmentation time, a fully-pixel-parallel cell-network-based architecture is suitable†. †T. Morimoto et al., 2nd COE Workshop, 2004.
- For cost-performance applications, in which real-time processing is not necessary, we propose image-scan video segmentation architecture.

Image-Scan Video Segmentation Architecture

- **High access-bandwidth embedded memories** for storing all inter mediate segmentation results of the complete image.
- **Image-scan approach** for segmentation processing with a small number of the processing elements.
- The proposed approach becomes very compact, it promises the possibility of hardware implementation with an FPGA.

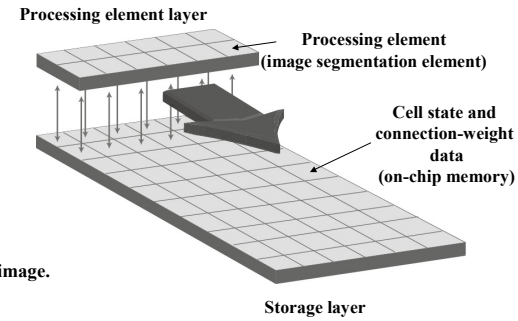


Fig. Conceptual diagram of image-scan video segmentation.

Video Segmentation Algorithm (Region Growing Approach)

Connection-weight calculation : Similarity of luminance between pixels
Leader cell selection : Sum of connection weights with neighboring pixels has to be larger than a threshold
Segmentation : Repeat self-excitation, excitation, and inhibition
Attach label : Result of the segmentation

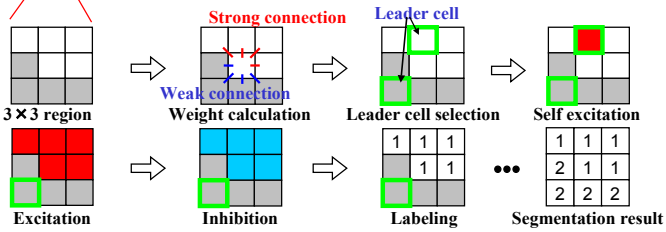


Image-Scan Video Segmentation Architecture

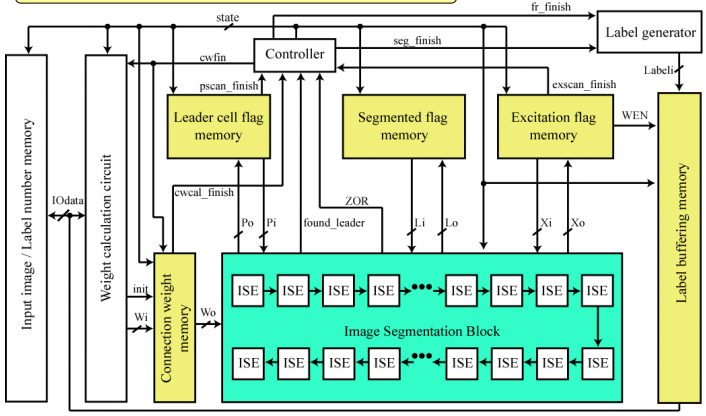
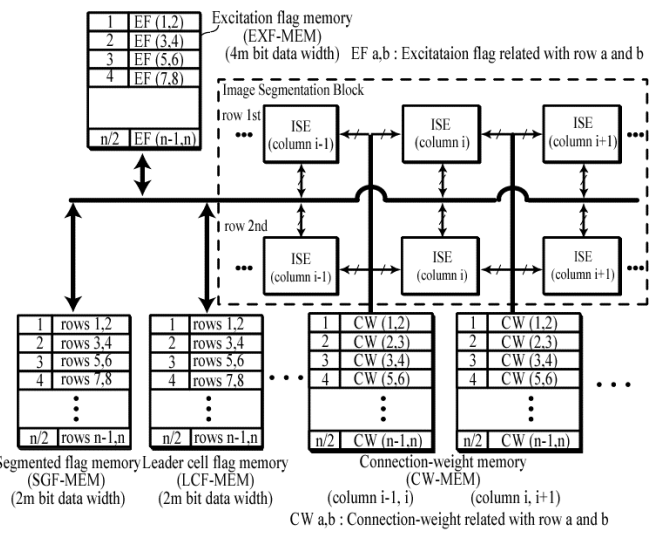


Fig. Block diagram of the row-scan based image segmentation architecture.

- The image-scan approach is implemented with an architecture consisting of **an embedded memory part** and **a processing part**.
- All status and connection-weight data for segmentation processing of m×2 pixels are stored under the same address in each on-chip memory, so that they can be accessed simultaneously in one clock cycle.



FPGA-Based Video Segmentation Prototype System

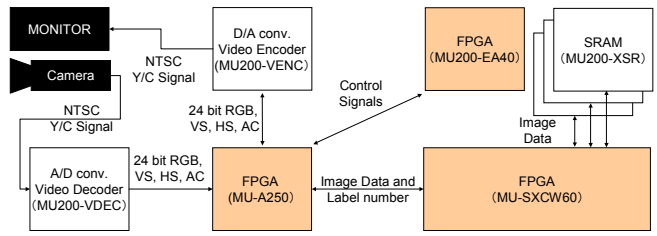


Fig. Conceptual diagram of image-scan video segmentation.

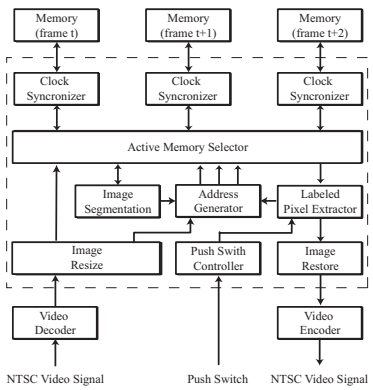


Fig. Block diagram of our segmentation evaluation system.

Three external memories are used for holding 3 frames, and this enables pipelining of the functions of transferring segmentation output display, processing in the image segmentation block, and image input from the video-camera.

Table System specification

Input/output format	NTSC Y/C signal
Number of pixels (image segmentation)	4,800 pixels (80x60 pixels)
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Code name	Magenta

Estimated Performance for QVGA size images


Walking man


Balls


Traffic

Table The usage of the logic elements and internal on-chip memory.

	Adaptive Look Up Tables (ALUTs)	Total memory bits
Proposed Architcture	78000	1.18Mbits
Target Device (FPGA Stratix Ⅱ)	143500	9.38Mbits
Ratio (%)	54%	19%

Table Clock cycles and processing time at 12MHz clock frequency, needed for the segmentation of the sample images with an FPGA implementation.

Segmented image	Clock cycle	Segmentation time @12MHz (msec/frame)
Walking man	2.7×10^5	20.25
Balls	1.9×10^5	10.58
Traffic	2.1×10^5	10.75

Conclusion

- A video segmentation architecture based on high bandwidth embedded memory and image scan approach has been proposed.
- An FPGA implementation verifies that QVGA size video segmentation on a single FPGA-chip becomes possible.
- The proposed architecture can be applied to large-scale image segmentation with compact hardware in real-time.