

# Influence of Bulk Bias on Negative Bias Temperature Instability of pMOSFETs with Ultrathin Plasma-Nitrided Gate Oxide

Shiyang Zhu, Anri Nakajima, Takuo Ohashi\* and Hideharu Miyake\*

Research Center for Nanodevices and Systems, Hiroshima University,  
1-4-2 Kagamiyama, Higashi-Hiroshima 739-8527, Japan,

\*Elpida Memory, Inc., 7-10 Yoshikawakogyodanchi, Higashi-Hiroshima 739-0198, Japan  
Phone: 81-824246274, Fax: 81-824243499, E-mail: [nakajima@sxsys.hiroshima-u.ac.jp](mailto:nakajima@sxsys.hiroshima-u.ac.jp)

## Introduction

The negative bias temperature instability (NBTI) of p-MOSFETs has become one of the most crucial reliability issues, especially when the gate oxide thickness is scaled down to less than 2nm and nitrogen is incorporated [1]. Considerable work has been done in both dc and ac NBT stresses, in which a voltage is applied on the gate electrode ( $V_g$ ) and the source/drain and substrate (bulk,  $V_b$ ) electrodes are grounded. It was reported that the positive bulk bias during the NBT stress has no influence on NBTI for  $V_b$  up to 4V [2,3]. But we find that the degradation can be enhanced significantly by  $V_b$ , and the enhancement depends on both  $V_g$  and  $V_b$ . Moreover, we find, for the first time, that the degradation can be dramatically enhanced under bipolar BT stress if the bulk electrode is floating. Both phenomena suggest that the interface trap generation during the BT stress is closely related to the tunneling of hole from Si to oxide, which can be enhanced by high  $V_b$  or the transient electrons in the channel (as well as trapped electrons in the interface states) during the bipolar BT stress with  $V_b$  floating.

## Experimental

The tested p-MOSFETs were fabricated on n-well of p-Si substrates using a standard CMOS process with LDD, P<sup>+</sup> poly gate, and plasma-nitrided gate oxide, which has a base oxide thickness of ~ 2nm and a peak nitrogen concentration of 9%. The device was stressed at 125°C, by applying a dc or ac voltage on the gate while source/drain grounded and the bulk electrode is grounded, positive biased or floating. The ac voltage has a square waveform of 50% duty factor and 4.5ns rise and fall time. Immediately after stress interruption, and  $I_d$ - $V_g$  and a modified direct-current current-voltage (DCIV) measurement [4] were carried out at the same temperature. Each stress was carried out on a fresh device whose initial interface trap density ( $N_{it}$ ) is between 1.5~ 3.0×10<sup>9</sup> cm<sup>-2</sup> for all tested devices.

## Results and Discussion

With increasing the stress time, the DCIV peak increases and the peak positive shifts to the negative direction, indicating the interface trap generation ( $\Delta N_{it}$ ) and the fixed oxide charge buildup ( $\Delta N_{ot}$ ) [4]. Figs. 1(a) and (b) show the threshold shifts

( $\Delta V_{th}$ ), which are extracted from the  $I_d$ - $V_g$  curves, and  $\Delta N_{it}$  data extracted from the DCIV peaks as a function of stress time under various  $V_g$  and  $V_b$ . Both figures show similar trends, i.e., at low  $|V_g|$  (1.5V),  $\Delta V_{th}$  (and  $\Delta N_{it}$ ) is almost independent of  $V_b$  (up to 2V), while at  $|V_g| \geq 2.0V$ , it is significantly enhanced at  $V_b = 2V$ . The enhancement magnitude depends on both  $V_g$  and  $V_b$ . The higher  $|V_g|$ , the lower  $V_b$  to trigger the enhancement is. It should be noted that the  $|V_b|$  value to trigger the enhancement is much lower than that reported by Y. Mitani *et al.* [3] and V. Huard *et al.* [2].

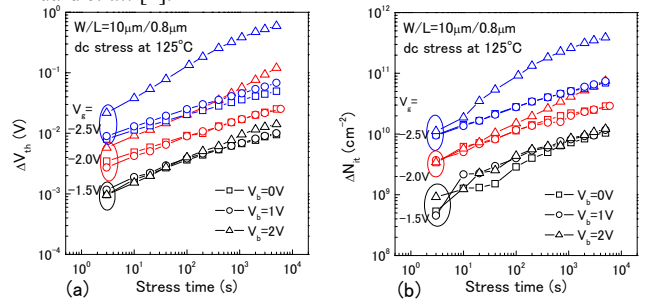


Fig. 1 (a)  $\Delta V_{th}$  and (b)  $\Delta N_{it}$  as a function of stress time under dc stress with various  $V_g$  and  $V_b$

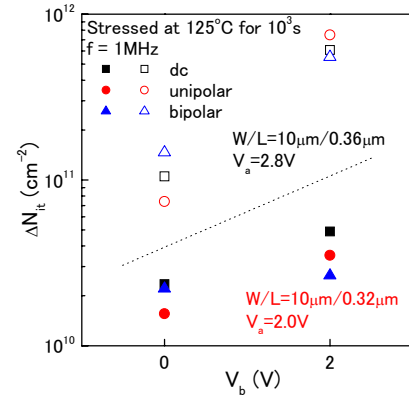
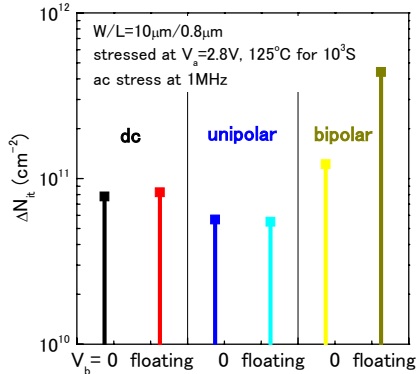


Fig. 2 The interface trap generation under dc, unipolar or bipolar pulsed stresses at  $V_b = 0$  or 2V. The magnitude of the stress voltage  $V_a$  is 2.0V or 2.8V.

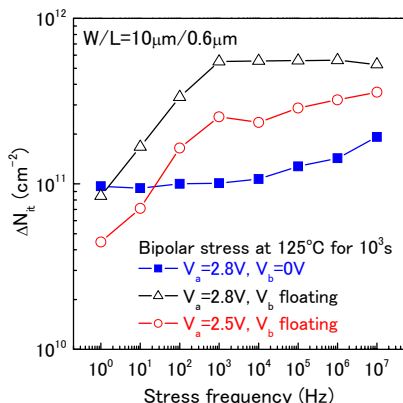
Fig. 2 shows the interface trap generation under dc and ac (both unipolar and bipolar) NBT stresses. Under ac NBT stress, similar  $V_b$  effect still exists, while the enhancement magnitude is slightly decreased under the bipolar stress. On the other hand, Fig. 3 shows that, with the bulk electrode floating,  $\Delta N_{it}$  is

dramatically enhanced under the bipolar stress while it remains almost unchanged under the dc or unipolar stress. The increase magnitude of  $\Delta V_{th}$  is larger than that of  $\Delta N_{it}$  (not shown here), indicating that  $\Delta N_{ot}$  is enhanced more significantly than  $\Delta N_{it}$ .

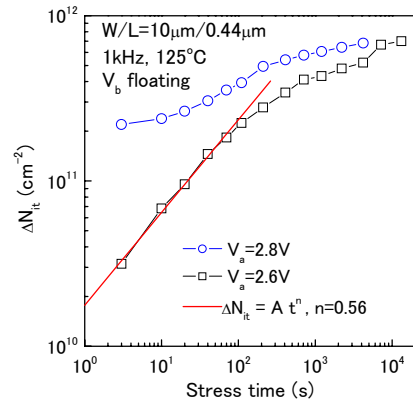


**Fig. 3** The interface trap generation  $\Delta N_{it}$  after static, unipolar or bipolar stress with  $V_b$  grounded or floating for 1000s. The degradation is dramatically enhanced under bipolar stress with  $V_b$  floating.

Fig. 4 shows the frequency dependence of interface trap generation under bipolar BT stresses with  $V_b$  floating. In normal bipolar BT stress ( $V_b=0$ ), the  $\Delta N_{it}$  enhancement occurs at frequency larger than  $\sim 10$  kHz [5-6]. With  $V_b$  floating, the enhancement magnitude is much larger and the enhancement occurs at 1 Hz and then saturates or increases very slowly at frequency larger than 1 kHz. Fig. 5 shows the time evolution of  $\Delta N_{it}$  under BT stress with  $V_b$  floating. At the early stress time,  $\Delta N_{it}$  increases with time in a power-law but with the exponent  $n$  much larger than 0.25, indicating that there is an additional mechanism for both  $\Delta N_{it}$  and  $\Delta N_{ot}$ . The decrease of the increase rate at the longer stress time, as well as the saturation trend in higher frequency region in Fig. 4, can be ascribed to the limited amount of the Si-H bonds at the  $\text{SiO}_2/\text{Si}$  interface [2].



**Fig. 4** The stress frequency dependence of interface trap generation  $\Delta N_{it}$  under bipolar BT stress with  $V_b$  floating or grounded. Devices with  $W/L = 10\mu\text{m}/0.6\mu\text{m}$  were stressed at  $125^\circ\text{C}$  for 1000s by a bipolar square waveform with  $V_a = 2.8\text{V}$  or  $2.5\text{V}$ . With  $V_b$  floating,  $\Delta N_{it}$  increases remarkably with frequency and then saturates at frequency larger than  $\sim 1\text{kHz}$ .



**Fig. 5** The time evolutions of the interface trap generation under bipolar BT stress with  $V_b$  floating and  $V_a = 2.6$  or  $2.8\text{V}$ . At the early stage of the  $V_a = 2.6\text{V}$  stress, a fitting line based on the power-law dependence is displayed.

It is well known that  $\Delta N_{it}$  (also  $\Delta N_{ot}$ ) is closely related to the holes in the inversion layer. We speculate that it is not the total density of holes, but the density of high-energy holes that can tunnel into oxide, plays a role to the  $\Delta N_{it}$  (and  $\Delta N_{ot}$ ). In the  $V_b = 0$  case, the holes are the “cold” holes, and are excited only by temperature. If  $V_b > 0$ , the holes can be accelerated by the bulk voltage, therefore the tunneling probability is significantly enhanced even though the total hole density is reduced due to the reduction of  $|V_g - V_{th}|$  [2]. In the case of bipolar stress with  $V_b$  floating, the channel electrons, as well as the electrons trapped at the interface can not follow the applied  $V_g$  variation if the transition time is less than about 1~10ms. The build-in electric field originated from these transient electrons can accelerate the hole tunneling, thus enhance the  $\Delta N_{it}$  generation.

Our finding indicates that, in some cases that the bulk electrode is floating, e.g. for SOI devices without body contact, a dramatic degradation may occur under bipolar stress. On the other hand, very large  $V_{th}$  shift (e.g.,  $>1\text{V}$ ) can be obtained at a relatively small  $|V_g|$  by floating  $V_b$  and applying a bipolar  $V_g$ .

## Conclusion

The  $V_b$  (grounded, positive biased, or floating) effects on both dc and ac NBTI are studied. The positive bulk bias can enhance the  $\Delta N_{it}$  generation significantly under dc and unipolar ac stresses. Moreover, a dramatic  $\Delta N_{it}$  enhancement is observed under the bipolar BT stress with  $V_b$  floating. We suspect that the enhancement is due to the enhanced tunneling probability, originated from the positive  $V_b$  or the transient electrons upon  $V_g$  reversal from positive to negative in the bipolar stress.

## Reference

- [1] D. K. Schroder and J. A. Babcock, *J. Appl. Phys.* **94** (2003) 1
- [2] V. Huard *et al.*, *Microelectronics Reliability* **45** (2005) 83
- [3] Y. Mitani *et al.*, *IEDM Tech. Dig.* (2002) 509
- [4] S. Zhu *et al.*, *Jpn J. Appl. Phys.* **44** (2005) L60
- [5] S. Zhu *et al.*, *IEEE Electron Device Letters*, **25**, (2005), 387
- [6] S. Zhu *et al.*, *IEEE Electron Device Letters*, **25**, (2005), 658

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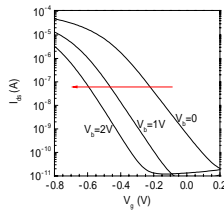
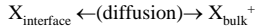
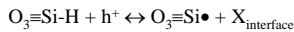
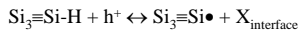
COE 2005, Hiroshima

## Outline:

- Background
- Experimental details
- Results:
  - $V_b$  positive bias
  - $V_b$  floating
- A model based on hot-hole injection
- Conclusion

## Background:

NBTI mechanism (Reaction-diffusion model):



### The role of holes?

The information can be obtained from the  $V_b$  effect.

$V_b \uparrow \rightarrow V_{th} \downarrow \rightarrow |V_g - V_{th}| \downarrow$   
 $\rightarrow$  channel hole density  $\downarrow$   
 $V_g$  fixed  $\rightarrow E_{ox}$  fixed

## Background (continuous):

### Static NBTI:

Contrary results in literature:

At the same  $V_g$ , no  $V_b$  effect up to  $V_b = 3V$ .

The lifetime decreases when  $V_b > 1.5V$ .

### Dynamic NBTI:

The degradation reduces under dynamic stress.

In our previous papers, degradation under bipolar BT stress is enhanced.

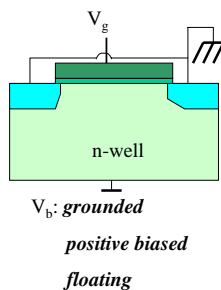
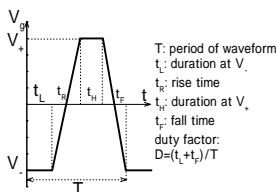
**No reports** about the  $V_b$  effect on dynamic NBTI.

## Experimental details:

**Devices:** pMOSFETs with p+ poly-Si gate, plasma-nitrided SiON gate.

$T_{ox} = 2.0\text{nm}$ ,  $N\% = 12\%$ ,  $W = 10\mu\text{m}$ ,  $L = 0.28 \sim 0.44\mu\text{m}$ .

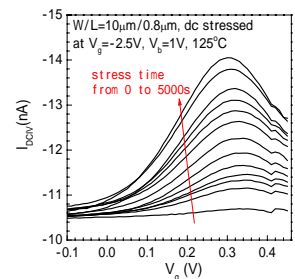
### Stress configuration:



## Measurement:

$I_d - V_g$  curves for  $V_{th}$ ;

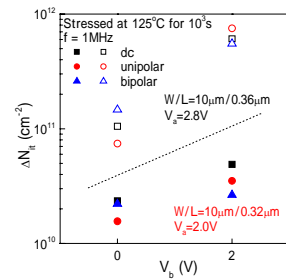
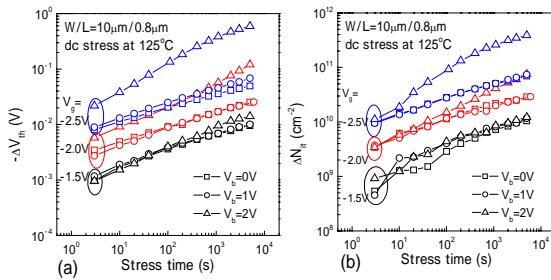
Modified DCIV (direct-current current-voltage) curves for  $N_{it}$ .



## Results:

### ----- $V_b$ positive bias

Device degradation under various  $V_g$  and  $V_b$ . The degradation enhancement depends on both  $V_g$  and  $V_b$ .

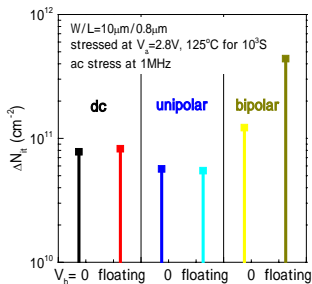


- At low  $V_g$ , the degradation is independent on  $V_b$  up to 2V.
- At high  $V_g$ , the degradation can be significantly enhanced by  $V_b$ .
- At dynamic stress with both unipolar and bipolar waveforms, similar  $V_b$  effect displays.

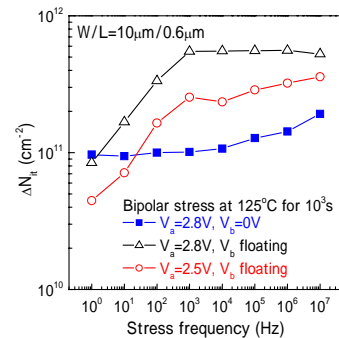
## Results:

### ----- $V_b$ floating

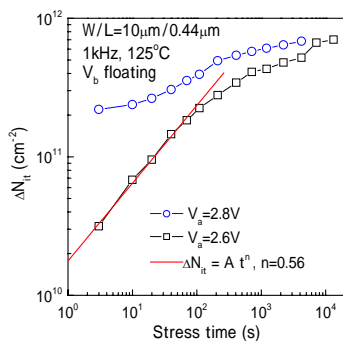
Under bipolar BT stress with  $V_b$  floating, the degradation is significantly enhanced.



Frequency dependence of degradation under bipolar stress with  $V_b$  grounded or floating.



Time evolution of degradation under bipolar BT stress with  $V_b$  floating



## Conclusion

- Significant degradation enhancement is observed by **applying a positive bulk bias** or by  **$V_b$  floating in the bipolar BT stress**.
- The degradation enhancement is attributed to an additional degradation related with the **hot hole injection**.
- The holes are energized by the electrical field provide by the positive bulk bias  $V_b$  or, in the case of bipolar BT stress with  $V_b$  floating, by the **transient electrons** in the channel upon  $V_g$  switched from positive to negative.