

## CONTENTS

### **PLENARY SESSION 9:00 – 16:40**

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*Reception Hall*, Faculty Club

9:00 **Welcome Remarks**

9:10 **Opening Address**

Taizo Muta, President, Hiroshima University

9:30 **Recent Progress of the COE**

Atsushi Iwata, COE Leader, Graduate School of Advanced Sciences of Matter, Hiroshima University

9:50 **[Invited] System LSI: Challenges and Opportunities**

Tadahiro Kuroda, Keio University

10:30 **[Invited] High-k Gate Dielectrics for Future CMOS Technology**

T. P. Ma, Yale University

11:10 **[Invited] Sub-20 nm Novel Silicon-Based Transistors**

J. C. S. Woo, UCLA

### **11:50 – 13:10 Lunch Break**

13:10 **[Invited] Perspective on Emerging Devices and their Impact on Scaling Technologies**

S. Biesemans, IMEC

13:50 **[Invited] Device Simulation for Nano MOSFET and Scaling Issues**

Y. J. Park, Seoul National University

14:30 **[Invited] Conventional Bulk and Bulk+ Architectures for 45 nm Node**

F. Boeuf, ST Microelectronics

### **15:10 – 15:20 Break**

15:20 **[Invited] Current Status of PVD Hf-Based High-k Gate Stack-Process Improvement on Drive**

**Current**

Masaaki Niwa, Matsushita Electric

16:00 **Current Activities in Device and Process R & D of the COE**

H. Sunami, S. Miyazaki, K. Shibahara, A. Nakajima, S. Yokoyama, and T. Kikkawa, Hiroshima University

**POSTER SESSION 16:40 –18:00**

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*Lounge*, Faculty Club

**P-01 A 3D Integration Architecture utilizing Wireless Interconnections for Implementing Hyper Brains**

Atsushi Iwata, Mamoru Sasaki, Takeshi Yoshida, Seiji Kameda, Hiroshi Ando, Masahiro Ono, Kan'ya Sasaki, Daisuke Arizono, and Takamaro Kikkawa

**P-02 A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip-Interconnect with Asynchronous Communication Scheme**

Mamoru Sasaki and Atsushi Iwata

**P-03 A brain-type vision system using a 3-dimensional integration with local and global wireless interconnections**

Seiji Kameda, Nobuo Sasaki, Daisuke Arizono, Masaki Odahara, Mamoru Sasaki, Takamaro Kikkawa, and Atsushi Iwata

**P-04 Robust Face Recognition Methods under Illumination Variations toward Hardware Implementation on 3DCSS**

H. Ando, N. Fuchigami, M. Sasaki, and A. Iwata

**P-05 A Layout Method of 20GHz Global Clock Distribution**

Mitsuru Shiozaki, Atsushi Mori, Atsushi Iwata, and Mamoru Sasaki

**P-06 A Robust Modular Learning Model with Addition and Integration of Modules**

Masahiro Ono, Mamoru Sasaki, and Atsushi Iwata

**P-07 A window-based stereoscopic system using a weighted average of costs aggregated with window size reduction**

Kan'ya Sasaki, Seiji Kameda, and Atsushi Iwata

**P-08 A CMOS RF Front-End using Radiation Oscillator for Short-Range Wireless Communication**

Toru Mukai, Atsushi Iwata, and Mamoru Sasaki

**P-09 A 1V Supply Low noise CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization**

Yoshihiro Masui, Takeshi Yoshida, Takayuki Mashimo, Mamoru Sasaki, and Atsushi Iwata

**P-10 Systems with Recognition and Learning Capability Based on Associative Memory**

Hans Juergen Mattausch and Tetsushi Koide

**P-11 Real-Time Multi-Object Tracking Based on Highly Parallel Image Segmentation and Pattern Matching**

Tetsushi Koide, Hans Juergen Mattausch, Takashi Morimoto, Hidekazu Adachi, and Kosuke Yamaoka

**P-12 Associative Memory Based Hardware Design for an OCR System and Prototyping with FPGA**

Ali Ahmadi, Md. Anwarul Abedin, Kazuhiro Kamimura, Yoshinori Shirakawa, Kazuhiro Takemura, Hans Juergen Mattausch, and Tetsushi Koide

- P-13 Fully-Parallel Associative Memory Architecture Realizing Minimum Euclidean Distance Search**  
Md. Anwarul Abedin, Kazuhiro Kamimura, Ali Ahmadi, Hans Juergen Mattausch, and Tetsushi Koide
- P-14 Image-Scan Video Segmentation Architecture Based on Embedded Memory Technology**  
Takashi Morimoto, Hidekazu Adachi, Kosuke Yamaoka, Tetsushi Koide, and Hans Juergen Mattausch
- P-15 CAM-Based Huffman Coding Architecture for Real-Time Applications**  
Takeshi Kumaki, Yasuto Kuroda, Tetsushi Koide, Hans Juergen Mattausch, Hideyuki Noda, Katsumi Dosaka, Kazutami Arimoto, and Kazunori Saito
- P-16 Unified Data/Instruction Cache with Distributed Crossbar, Hidden Precharge Pipeline and Dynamic CMOS Logic**  
Koh Johguchi, Zhaomin Zhu, Ken-ichi Aoyama, Yuya Mukuda, Hans Juergen Mattausch, Testushi Koide, and Tetsuo Hironaka
- P-17 Time-Domain-Based Modeling of Carrier Transport in Lateral p-i-n Photodiode**  
G. Suzuki, K. Konno, D. Navarro, N. Sadachika Y. Mizukane, O. Matsushima, T. Ezaki, Mitiko Miura-Mattausch, and S. Yokoyama
- P-18 Shot Noise Modeling in MOSFETs under Sub-threshold Condition**  
Yoshioki Isobe, Dondee Navarro, Youichi Takeda, Kiyohito Hara, Tatsuya Ezaki, and Mitiko Miura-Mattausch
- P-19 Wireless interconnects for UWB signal transmission in ULSIs Interconnection**  
T. Kikkawa, N. Sasaki, P. K. Saha, K. Kimoto, and M. Nitta
- P-20 The Development of UWB Gaussian Monocycle Pulse Synchronization Circuit based on 0.18 μm CMOS Technology**  
Nobuo Sasaki, Pran Kanai Saha, and Takamaro Kikkawa
- P-21 Effect of Supercritical Fluid Extraction Process on Self-assembled Porous Silica Films**  
Kouji Isari, Nobuyuki Kawakami, Yoshito Fukumoto, and Takamaro Kikkawa
- P-22 Impulse-based UWB transmitter in 0.18 μm CMOS for wireless interconnect in future ULSI**  
P. K. Saha, N. Sasaki, and T. Kikkawa
- P-23 Data Transmission Characteristics of Integrated Linear Dipole Antennas for UWB Communication in Si ULSI**  
K. Kimoto, N. Sasaki, M. Nitta, and T. Kikkawa
- P-24 Interference of Digital Noise with Integrated Dipole Antenna for Inter-chip Signal Transmission In ULSI**  
M. Nitta and T. Kikkawa
- P-25 Front-End Technologies for nano-scale MOSFETs**  
Kentaro Shibahara
- P-26 Workfunction Tuning of Fully-Silicided NiSi Gate with Poly-Si Predoping**  
Takuji Hosoi, Kousuke Sano, Masaki Hino, Norihiro Ooishi, and Kentaro Shibahara

**P-27 Development of Three-Dimensional Beam-Channel MOS Transistors**

Hideo Sunami, Kei Kobayashi, Shunpei Matsumura, Koji Yoshikawa, and Kiyoshi Okuyama

**P-28 Constraint of Source/Drain Formation with Plasma Doping Applied for Beam Channel Transistor on SOI**

Kei Kobayashi, Kiyoshi Okuyama, Koji Yoshikawa, and Hideo Sunami

**P-29 Characterization of Newly Developed 3-D Parallel-Triple Gate MOS Transistor**

Kiyoshi Okuyama, Koji Yoshikawa, and Hideo Sunami

**P-30 Control of Charged States of Silicon Quantum Dots and Their Application to Floating Gate MOS Memories and Light Emitting Diodes**

Seiichi Miyazaki

**P-31 Impact of Rapid Thermal Annealing on ALCVD-Al<sub>2</sub>O<sub>3</sub>/Si<sub>3</sub>N<sub>4</sub>/Si(100) Stack Structures --Photoelectron Spectroscopy**

H. Murakami, F. Takeno, A. Ohta, S. Higashi , S. Miyazaki, K. Komeda, M. Horikawa, and K. Koyama

**P-32 Formation of Si Nano-crystals by Millisecond Annealing of SiO<sub>x</sub> Films using Thermal Plasma Jet**

Seiichiro Higashi, Tatsuya Okada, Noto Fujii, Naohiro Koba, Hideki Murakami, and Seiichi Miyazaki

**P-33 Fabrication of Multiply-Stacked Structures Consisting of Si-QDs with Ultrathin SiO<sub>2</sub> and Its Application of Light Emitting Diodes**

Katsunori Makihara, Yoshihiro Kawaguchi, Hideki Murakami, Seiichiro Higashi, and Seiichi Miyazaki

**P-34 Characterization of Electronic Charged States of P-doped Si Quantum Dots Using AFM/Kelvin Probe**

Katsunori Makihara, Hideki Murakami, Seiichiro Higashi, and Seiichi Miyazaki

**P-35 Characterization of Charge Trapping and Dielectric Breakdown of HfAlO<sub>x</sub>/SiON Dielectric Gate Stack**

Yanli Pei, Satoru Nagamachi, Hideki Murakami, Seiichiro Higashi, Seiichi Miyazaki, Takaaki Kawahara, Kazuyoshi Torii, and Yasuo Nara

**P-36 Characterization of Chemical Bonding Features of NH<sub>3</sub>-Annealed Hafnium Oxides Formed on Si(100)**

H. Nakagawa, A. Ohta, H. Murakami, S. Higashi, and S. Miyazaki

**P-37 XPS Study of Ultrathin GeO<sub>2</sub>/Ge System**

Akio Ohta, Hiroaki Furukawa, Hiroshi Nakagawa, Hideki Murakami, Seiichiro Higashi, and Seiichi Miyazaki

**P-38 Phase Transformation of Amorphous Si Films in Millisecond Time Domain Induced by Thermal Plasma Jet Irradiation**

H. Kaku, S. Higashi, T. Okada, H. Murakami, and S. Miyazaki

**P-39 Characterization of Multi Step Electron Charging to Silicon-Quantum-Dot Floating Gate by Applying Pulsed Gate Biases**

T. Nagai, M. Ikeda, Y. Shimizu, S. Higashi, and S. Miyazaki

**P-40 Decay Characteristics of Electronic Charged States of Si Quantum Dots as Evaluated by an AFM/Kelvin Probe Technique**

Junichiro Nishitani, Katsunori Makihara, Mitsuhsia Ikeda, Hideki Murakami, Seiichiro Higashi, and Seiichi Miyazaki

**P-41 Analysis of Transient Temperature Profile During Thermal Plasma Jet Annealing of Si Films on Quartz Substrate**

T. Okada, S. Higashi, H. Kaku, N. Koba, H. Murakami, and S. Miyazaki

**P-42 Status of Research on Optical Interconnection in LSI**

Shin Yokoyama

**P-43 Design and Simulation of Ring Resonator Optical Switches using Electro- and Magneto-Optic Materials**

Yuichiro Tanushi and Shin Yokoyama

**P-44 Groove-Buried Optical Waveguides Based on Metal Organic Solution-Derived  $\text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3$  Thin Films**

Zhimou Xu, Masato Suzuki, Yuichiro Tanushi, Keita Wakushima, and Shin Yokoyama

**P-45 Structural and Optical Properties of Electro-Optic Material: Sputtered  $(\text{Ba},\text{Sr})\text{TiO}_3$**

Masato Suzuki, Zhimou Xu, Yuichiro Tanushi, and Shin Yokoyama

**P-46 Integration of High-Speed Photodetectors on Si LSI**

Masayuki Kitaura, Yoshio Mizukane, Shin Yokoyama, and Mitiko Miura-Mattausch

**P-47 Development of Photodetectors using Si Quantum Dots**

Mitsuhsia Ikeda, Masayuki Kitaura, Seiichi Miyazaki, and Shin Yokoyama

**P-48 Fabrication of Spin-Coat Optical Waveguides for Optically Interconnected LSI and Influence of Fabrication Process on Lower Layer MOS Capacitors**

Tetsuo Tabei, Kazuhiko Maeda, Shin Yokoyama, and Hideo Sunami

**P-49 Smooth Cu Thin Film Fabricated by  $\text{H}_2$  Addition Sputtering**

Masahiro Ooka and Shin Yokoyama

**P-50 Characterization and application of SiON gate dielectrics**

Anri Nakajima, Shiyang Zhu, Takuo Ohashi, and Hideharu Miyake

**P-51 Infuence of Bulk Bias on Negative Bias Temperature Instability of pMOSFETs with Ultrathin Plasma-Nitrided Gate Oxide**

Shiyang Zhu, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake

**P-52 [Invited] Dynamic Behavior of Human Eye**

Roland Kempf, Yuichi Kurita, Yoshichika Iida, Makoto Kaneko, Hiromu Mishima, Hidetoshi Tsukamoto, and Eiichiro Sugimoto

