21st Century COE Program

The Fifth International Workshop on
Nanoelectronics for Tera-Bit Information Processing

Technology Challenges for Future CMOS

Masataka Hirose
MIRAI, Advanced Semiconductor Research Center(ASRC)
National Institute for Advanced Industrial Science and Technology (AIST)

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Presentation Overview

1. Technology Shift from Traditional Scaling
2. Carrier Transport Enhancement in MOSFET
    - Strain
    - Channel Materials
    - FET Architecture
3. Metal/High-k Gate Stack Technology
    - Vth Tuning and FLP
    - Gate Effective WorkFunction and FLP Mechanism
4. Future Direction/Challenges

Acknowledgements

A. Toriumi, MIRAI-AIST, The University of Tokyo
S. Takagi, MIRAI-AIST, The University of Tokyo
T. Kanayama, MIRAI-AIST

All the colleagues of High-k and Transistor Groups
in the MIRAI Project

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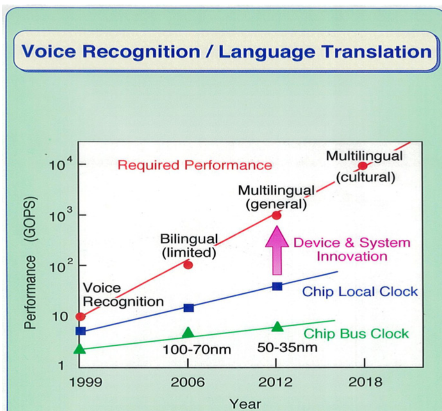
Aggressive Investment Continuing in Global Semiconductor Industries

Tsugio Makimoto
"Nation's Future and Semiconductors"

- Semiconductor Market in Japan US$50B
- Impact to GDP US$2T(40% of GDP)

Escalating Needs for Information Processing



3D Real Time Graphics also Needs 10^3GOPS.

Human Communicator Electronics WG(1999)

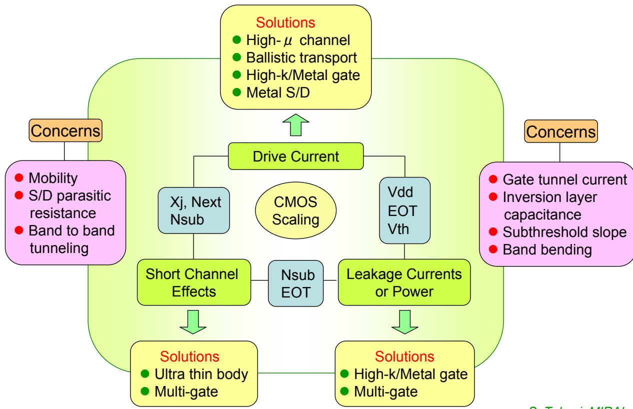
Moore's Law is Evolving through Technology Shift from Traditional Scaling

No Exponential is Forever : But"Forever" Can be Delayed!
G. Moore, ISSCC 2003

- Number of Transistors (Shrinking printed dimensions / growing die size)
    - Annual Doubling(1965)
    - Two-year Doubling(1975)
- Change in Scaling Scenario
    - 0.5 μm CMOS performance was mostly achieved by conventional scaling.
    - In 90 nm CMOS, 60% of the performance is achieved by introducing new technologies, while 40% by extension.

B. Meyerson, ISSM 2004

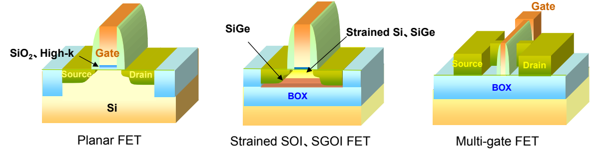
Trade-off Factors in Device Scaling



S. Takagi, MIRAI

New Materials and Structures for MOSFET

MOSFET Evolution → 2015



Planar FET — Strained SOI、SGOI FET — Multi-gate FET

Materials Evolution

	Present		Future
Channel	Si	→	High-μ Materials (Strained Si, SiGe, Ge)
Gate Dielectrics	SiO2(SiON)	→	High-k Dielectrics (HfSiO, HfAlO, LaAlO)
Gate Electrode	Poly-Si	→	Metal, Metal Silicide
Source/Drain	Si	→	SiGe, MSi_x, MGe_x

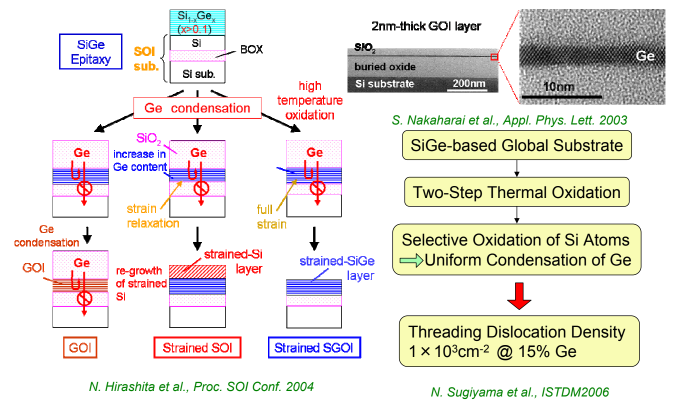
Keeping Ioff low and enhancing Ion by optimal selection of materials and structures

Technology Challenges for Future CMOS

2. Carrier Transport Enhancement in MOSFET

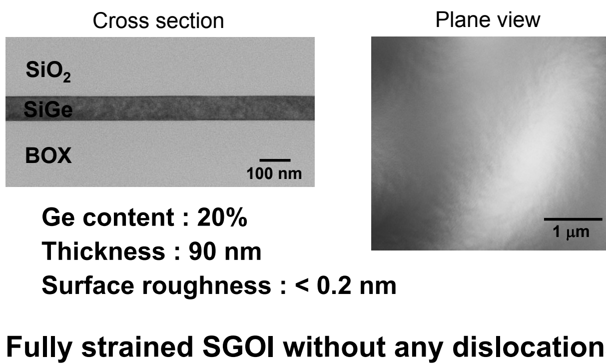
- Subband Structure Engineering with :
  - Strain (Uni-axial, Bi-axial)
  - Channel Materials (Si, SiGe, Ge)
  - Surface Orientation
  - Multi-gate Architecture

SSOI, SGOI and GOI Wafer Technology



TEM Images of Fully Strained SGOI Substrate

Cross section — Plane view



Ge content : 20%

Thickness : 90 nm

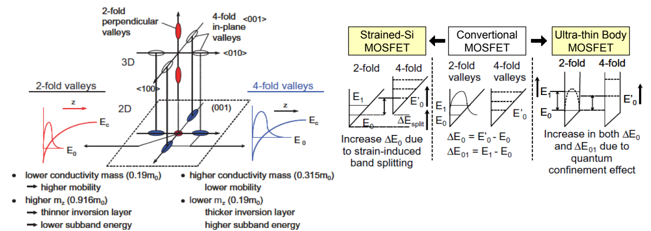
Surface roughness : < 0.2 nm

Fully strained SGOI without any dislocations

Subband Structure Modulation with Tensile Strain

Ground states of the 2- and 4-fold valleys for 2-dimensional electrons in Si (100) surface inversion layer.

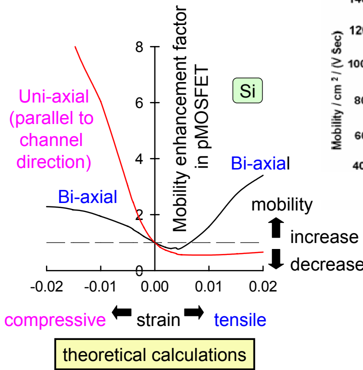
Subband structure engineering for increasing the occupancy of 2-fold valley (higher μ)electrons.



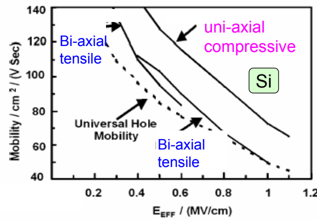
S. Takagi et al., IEDM1997
S.Takagi et al., Solid State Electr. 49(2005)684

IRAI Hole Mobility Enhancement due to Bi- and Uni-axial Strain

M. Uchida et al., Proc. SISPAD (2005) p.315



T. Ghani et al., IEDM 2003



- Uni-axial compressive (Induced by SiGe S/D Epi or SiN liner) Beneficial to pFET
- Tensile strain benefits nFET mobility

IRAI Mobility Anisotropy of Electrons and Holes in MOSFET Inversion Layer

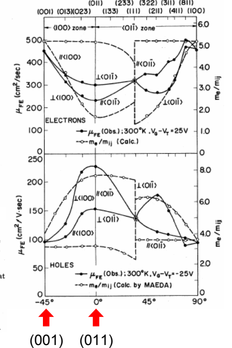
PHYSICAL REVIEW B VOLUME 4, NUMBER 6 15 SEPTEMBER 1971

Mobility Anisotropy of Electrons in Inversion Layers on Oxidized Silicon Surfaces

Tai Satô, Yoshiyuki Takeishi, and Hisashi Hara
Toshiba Research and Development Center, Tokyo Shibaura Electric Company, Ltd., Komukai, Kawasaki, Japan
and
Yoshihiko Okamoto
I. C. Engineering Department, Tokyo Shibaura Electric Company, Ltd., Komukai, Kawasaki, Japan
(Received 10 December 1970)

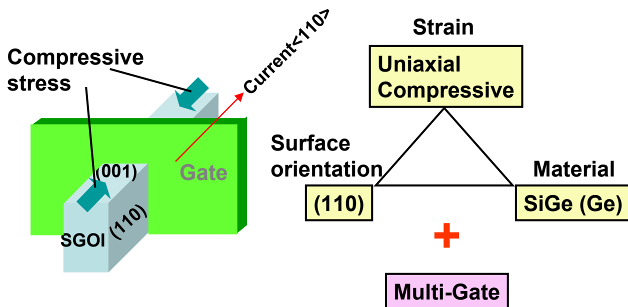
Measurements of the field-effect mobility of electrons in n-type inversion layers of Si as functions of the crystalline orientation of the surface and of the azimuthal direction of the current path within the layers are reported. Significant mobility anisotropy observed over a range of strong electric fields perpendicular to the surface at temperatures from 77 to 320 °K contrasts substantially with that in the case of p-type inversion layers reported previously. The anisotropy at room temperature can be successfully interpreted in terms of the effective-mass anisotropy calculated on the basis of Stern and Howard's formula for the two-dimensional carriers. For a full understanding of the experimental results, particularly at low temperatures, theoretical investigations including the anisotropy of the relaxation time are required, but have not been explored enough. Extensive data on the dependences of the mobility on the electric field and temperature as well as bulk-acceptor concentration are presented and discussed in the light of existing scattering theories. Some hole-mobility data are included for comparison.

FIG. 2. Plots of the field-effect mobility of electrons (upper half) as functions of surface orientation and current-flow direction. The calculated reciprocal effective mass of electrons in the lowest subband (see Table II) is also plotted by dotted lines. Corresponding results (Ref. 1) of hole mobility are reproduced for comparison (lower half). The apparent discontinuity of the masses at the (111) [and p channel (100)] surfaces comes from the fact that only the lowest subband is considered. Near the (111) surface, the energy of upper subbands comes closer and closer to the energy of the lowest subband. If the population into these upper subbands is taken into account statistically, these discontinuities should disappear (see Table III).



T. Sato et al., Phys. Rev. B, 4(1971)1950
T. Sato et al., Jpn. J. Appl. Phys 8(1969)588

IRAI Multi-Gate pMOS with Uniaxially-Strained SGOI Channels

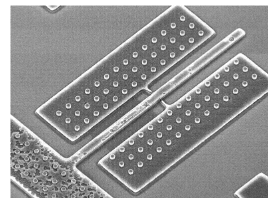


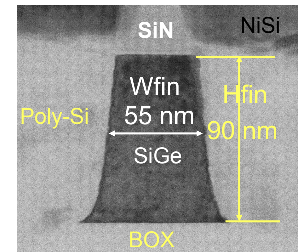
All performance enhancement boosters for pMOS can be adequately combined.

IRAI Fabricated Strained SGOI FinFET

1.6 nm SiON gate oxide
Ni SALICIDE

Cross Sectional TEM

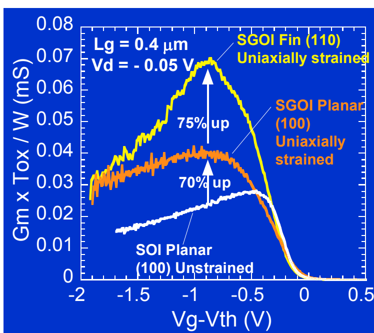




Good crystal quality has been maintained even after device fabrication processes.

T. Irisawa et al., IEDM 2005

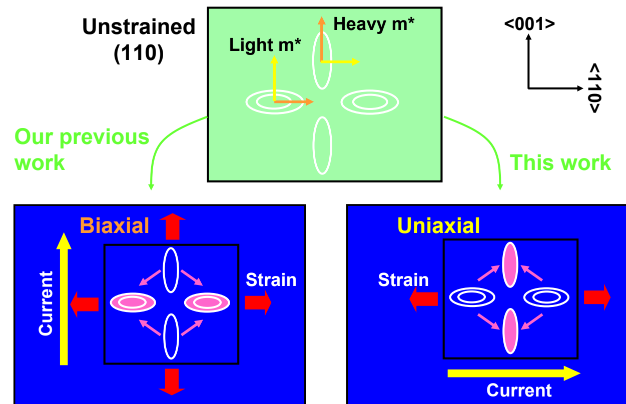
IRAI Gm Enhancement in Uniaxially Strained, SGOI(110) Fin FET



Large g_m enhancement due to uniaxial compressive stress as well as (110) surface orientation.

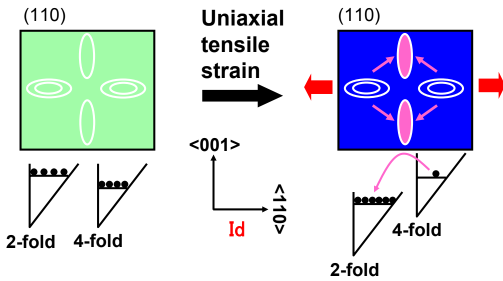
T. Irisawa et al., IEDM 2005

IRAI Subband Engineering for (110) nMOS



T. Mizuno et al IEEE EDL 41. pp.266 (2003).

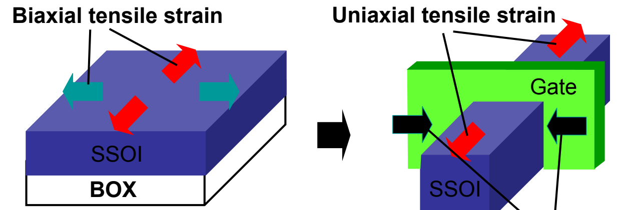
IRAI Advantages of Uniaxial Strain in (110) nMOSFET



1) 2-fold valleys is occupied (light m*, m* reduction[1])
2) Optimum current direction is the same as pMOS
3) Good compatibility with multi-gate structures
(as shown next)

[1] K. Uchida et al., IEDM. (2005).

IRAI Uniaxially Strained Device Structure Fabricated from SSOI



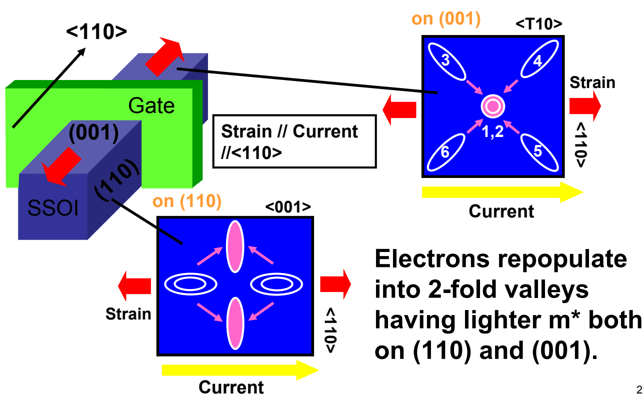
Single-layer strained SOI sub.
(40 nm re-growth on 15 nm initial sub.)
Strain = 0.9% (Biaxial)

Strain relaxation

T. Irisawa et al., *IEDM* (2005)
N. Collaert et al., *VLSI* symp. (2006)

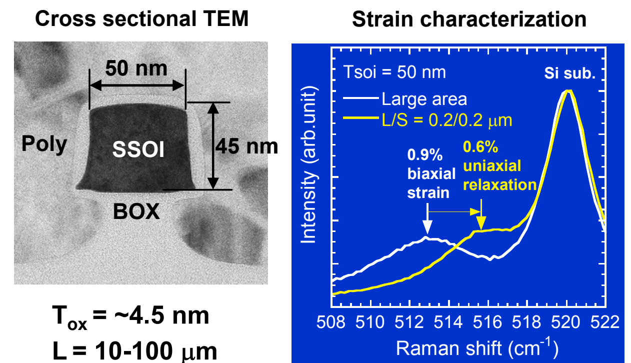
Uniaxial tensile strain along current flow direction is applied by lateral strain relaxation

IRAI Subband Engineering by Uniaxial Strain in Tri-gate MOSFET



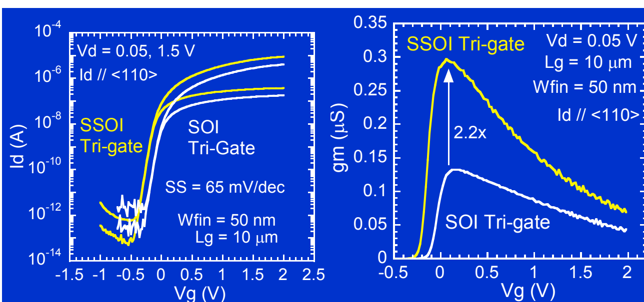
Electrons repopulate into 2-fold valleys having lighter m* both on (110) and (001).

IRAI Fabricated Tri-gate MOSFET



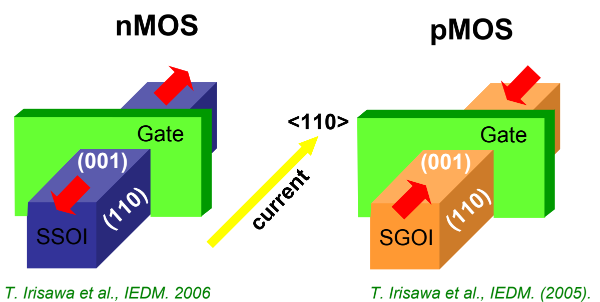
T_{ox} = ~4.5 nm
L = 10-100 μm

IRAI Id-Vg and gm Characteristics



Large gm enhancement of 2.2x is observed in SSOI Tri-gate

IRAI Uniaxially Strained CMOS with Optimally Designed Subband Structures



T. Irisawa et al., IEDM. 2006

T. Irisawa et al., IEDM. (2005).

Optimum multi-gate CMOS structure is realized on the same (001) wafer along the same <110> direction

Technology Challenges for Future CMOS

3. Metal/High-k Gate Stack Technology

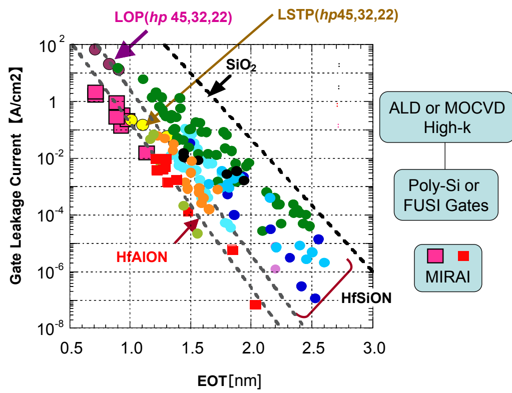
- High-k Performance and Mechanism
  - Gate Leakage and Channel Mobility
  - Vth Tuning and FLP
  - Gate Effective Workfunction
  - FLP Mechanism

Metal Gate/High-k Gate Stack Technology

	nMOS	pMOS
Metal	TaC, NiSi, HfSi, Ta(Tb, Er, Yb)N, (Ta, Hf, Mo)SiN	Pt, Ru, Re, $PtSi_x$, Ni_3Si, MoN_x, TiSiN, TiCN
Top Layer	La_2O_3	Al_2O_3, AlN
High-k	HfLaO	HfAlO
	HfSiO(N), HfO_2	
Si sub.	N I/I	F I/I

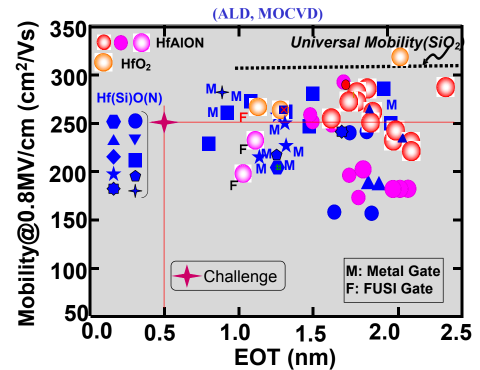
VLSI2005, VLSI2006, IEDM2004, IEDM2005

Gate Tunneling Leakage Current Benchmark



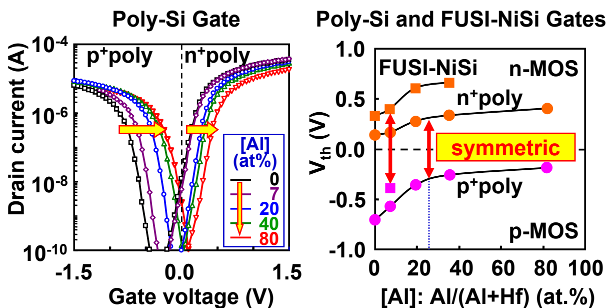
A. Toriumi et al., Microelectronic Engn. 2005

High-k MOFET Mobility Benchmark



Ref : VLSI Tech. Symp. 2003-2006, IEDM, 2003-2005, SSDM 2005

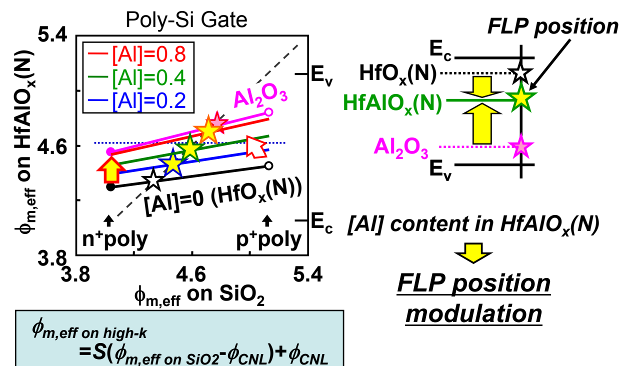
V_{th} Tuning with Al Content in $HfAlO_x$(N)



- Symmetric V_{th} can be obtained at [Al] 25 at.% for poly-Si and ~7 at.% for FUSI-NiSi.

M. Kadoshima et al., VLSI Symp. 2005 p.70

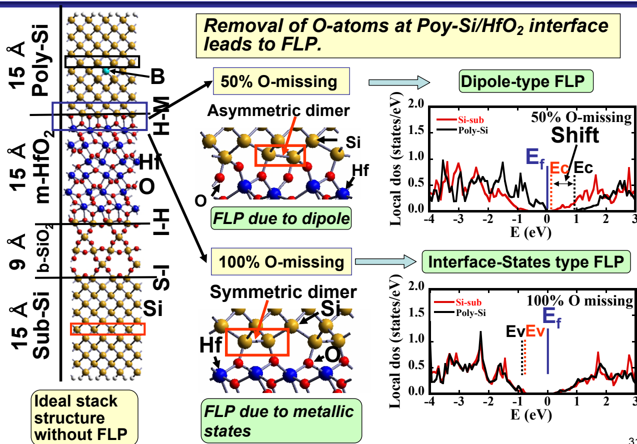
FLP Position Modulation with Al Content in $HfAlO_x$(N)



$$\phi_{m,eff\ on\ high\text{-}k} = S(\phi_{m,eff\ on\ SiO2} - \phi_{CNL}) + \phi_{CNL}$$

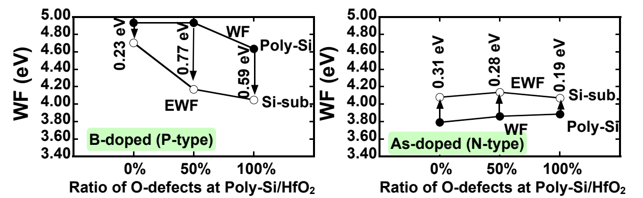
M. Kadoshima et al., VLSI Symp. 2005 p.70

IRAI The First Principles Analysis of FLP in Poly-Si/HfO_2



IRAI Effective Workfunction of Poly-Si

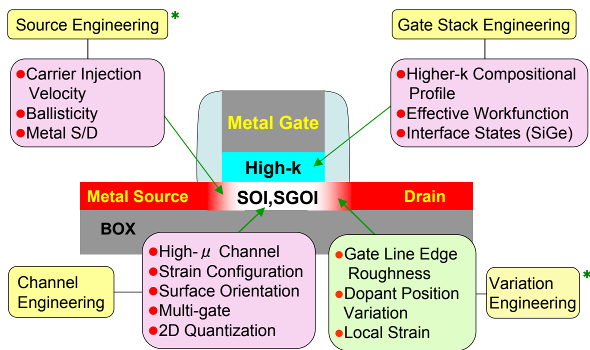
By removing O-atoms at Poly-Si/HfO_2 interface, we obtain WF and EWF for p- and n-type Poly-Si on HfO_2.



- p-type electrode: EWF tends to decrease by 0.6～0.8eV.
- n-type elctrode: EWF tends to increase by 0.3～0.2eV.

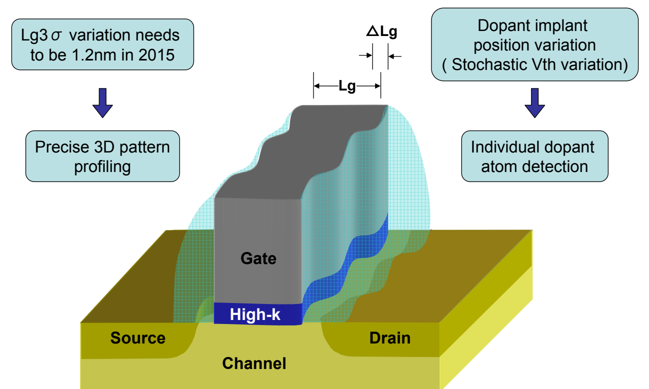
First principles calculations well describe FLP consistently.

IRAI Future Direction/Challenges

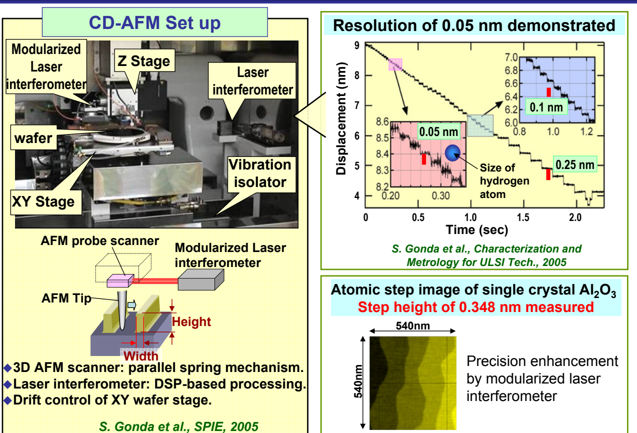


Device Engineering for Implementing New Materials and Structures

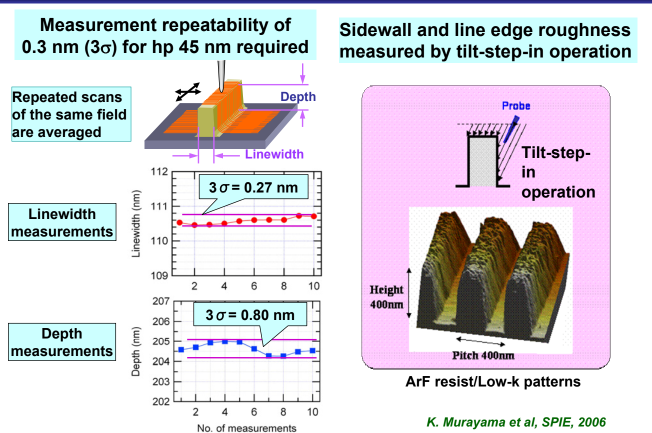
IRAI Gate Line Edge Roughness and Channel Dopant Position Variation



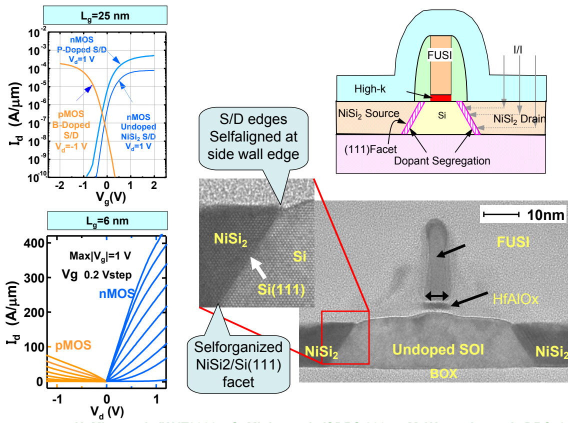
IRAI High-Precision CD Metrology by AFM



IRAI Three-Dimensional Metrology by CD-AFM

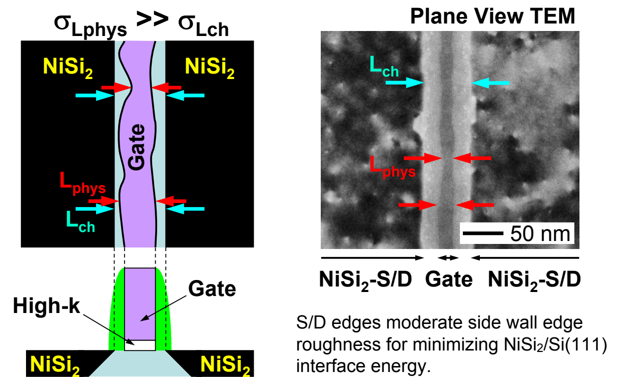


IRAI Metal/High-k, Epitaxial $NiSi_2$ S/D, UTB SOI MOSFET



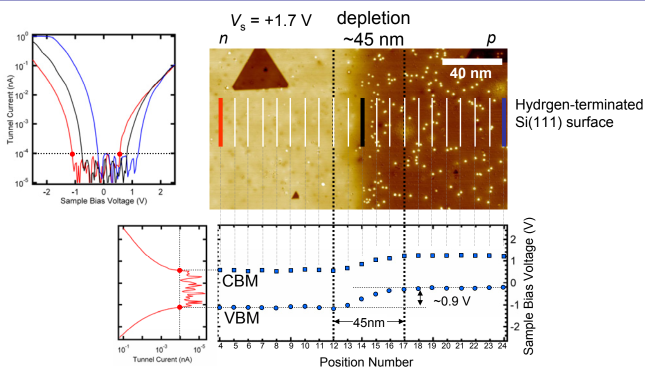
N. Mise et al., IWJT2006, S. Migita et al., ISDRS 2005, M. Watanabe et al., DRC, 2005

IRAI L_{ch}-Variation Suppression by Epitaxial S/D



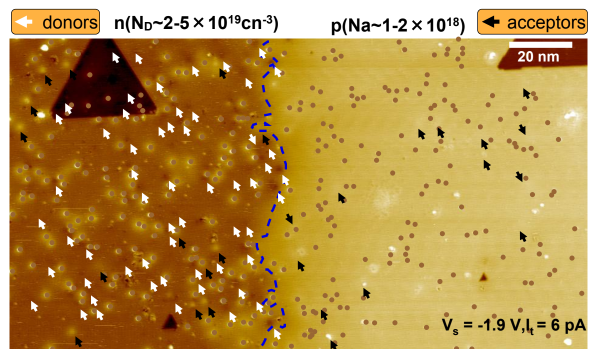
S/D edges moderate side wall edge roughness for minimizing $NiSi_2$/Si(111) interface energy.

IRAI High-Spatial-Resolution Potential Profile of pn Junction by STM



Depletion layer width obtained from potential simulation agrees with the measured value.

IRAI Individual Dopant Distributions and Potential Fluctuations in pn Junction



Donor distribution correlates with the local potential fluctuation.

M. Nishizawa et al., SSDM2006

IRAI SUMMARY

Back to Science for Future CMOS Technology and Beyond

- Subband structure engineering with strain configuration, channel materials, surface orientation and FET architecture is a key to enhance CMOS performance.
- Atomic level understanding and control of high-k gate stack interfaces including high-k compositional profile design are needed.
- Materials science for high-μ channels and higher-k gate dielectrics, and new concept of angstrom metrology which meet the future industry needs are great challenges.