

# Summary of the 21st COE Program on Nanoelectronics for Tera-bit Information Processing

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## 1. Target of the COE

The COE program on “Nano-electronics for Tera-bit Information Processing” has focused on research collaboration in 3 fields of (1) circuit design and system architecture, (2) principle and simulation program for future MOS devices model, and (3) structures, materials and processing of nano-devices. (Fig. 1) We aimed at novel system architecture and design method utilizing scaled nano-devices, new device structures predicted by physical modeling, and new materials based on quantum physics. The main target is to achieve the technology innovation for implementing hyper brain systems with tera-bit information processing capability.

## 2. Research Subjects

Device modeling is the key to organize research collaboration between the field of circuit/system and device/process. the accurate device model enables highly sophisticated circuit design such as the wireless transceiver f with low power dissipation. In order to integrate tera-bit information processing systems, we have to develop ultimately scaled MOS devices with novel structures, integrated antennas, optical components, and their fabrication process technologies including novel materials. In these fields, device modeling is effective to predict prospective function and performance of devices. Research on multi-layered Si quantum dot structure will result in new optical memory devices. By the synergy between these researches, the innovative 3-D integration have been developed for the target of tera-bit information processing.

In order to realize human like brain system which can recognize various objects in real-time/real-world, numbers of chips with massively parallel processing and wideband interconnection capabilities, are required. (Fig. 2) To solve the problem, we have proposed the 3-dimensional integration technology using wireless interconnections instead of bonding wires or via holes. <sup>[1]</sup>(Fig. 3)

## 3. COE formation and education

### [Research cooperation]

The design and measurement of the 3-D integration prototype has performed by cooperation with the members of circuit/system and device/process fields. Key points are (1) the architecture of image processing system utilizing the

features of wireless interconnections and (2) the design of RF transceiver including integrated antennas and inductors using various kinds of electro-magnetic analysis. The research on new device structures and materials and fabrication technologies aiming at 3-D integration has also progressed. Thirteen postdoctoral researchers and 21 doctoral course students have actively worked in the COE.

HiSIM Research Center was established in Hiroshima University in June, 2005. The center has been working on development of the family of HiSIM models aiming at standard models for Bulk, SOI, and DMOS devices.

### [Education system]

We established the new department of “Semiconductor Electronics and Integration Sciences”, in April 2004, in the Graduate School of Advanced Sciences of Matter, Hiroshima University. We have practiced new education programs through advanced research and practical training. Moreover, 10 students per year attended the internship program at semiconductor and IT companies. As the results of intensive education program, we have given the doctoral degree to 31 candidates and the master’s degree to 128 students from 2003 to 2007.

### [Publicity]

For publicity of the COE achievement, we held the international workshop on nano-electronic once a year from 2003. This is the fifth workshop for reporting the final achievements of our COE program.

## 4. MOSFET Modeling Technique

Profs. Miura has developed *HiSIM* model for scaled MOSFETs described by the surface potential based on drift and diffusion. *HiSIM2* including Non-Quasi-Static effects realizes sufficient accuracy in noise and distortion at GHz RF circuit operation. The Compact Model Council selected *HiSIM* as the final stage candidate for the standard model in March, 2005. Although *PSP* model was selected as the standard or bulk MOS devices in the end of 2005, study for SOI and DMOS device models has continued.

Moreover, Prof. Miura has developed a photodiode model for circuit simulation, considering the transient carrier generation explicitly in the solution of the continuity equation. The electric field distribution along depth direction of the PD is found to cause a tail in the photo current, which has adverse effects on optical response of PDs. <sup>[2]</sup>(Fig. 4)

## 5. Circuit and System

### 5.1 Wireless Interconnections

#### [Wireless interconnect using on-chip antennas]

Prof. Kikkawa has proposed a new inter-chip and intra-chip connection technique using electro-magnetic wave propagation using on-chip antennas. They have confirmed by measurements that antenna transmission gain is about -28dB at 20GHz, and it decreases only 0.14dB/chip with 270 $\mu$ m chip thickness. We call this technique Global Wireless Interconnection (*GWI*) which is applicable to clock distribution and data busses between whole chips.<sup>[3]</sup>

The IR-UWB transmitter with integrated antenna has been developed. (Fig. 5) The transmitter consists of GMP generator, amplifiers, a source follower and an integrated dipole antenna. The GMP circuits are composed of 8 stage voltage controlled oscillator, 8-1 multiplexer, triangular pulse generation (TPG) and differentiator. A test chip was fabricated in 0.18  $\mu$ m CMOS technology. The measured GMP after the differentiator has 123mVpp amplitude and 280 ps pulse width. GMP center frequency was 3.6GHz at 1.8V. The transmitted signal was measured after source follower by using SS probe and barn. The communication of the GMP at 1 mm distance in Si substrate by the integrated dipole antennas was successfully demonstrated for the first time.<sup>[4]</sup> A pulse repetition rate of 1.16 Gbps was transferred. The total power dissipation of the transmitter is 21.6mW at 1.8V.

#### [Wireless interconnects using on-chip spiral inductors]

Prof. Iwata and Sasaki have proposed wireless interconnection using on-chip spiral inductor pair for neighboring chip connection. Resonance phenomena of inductor pair are utilized for reducing dissipation power and increasing bit rate with a simple transmitter and receiver. (Fig.6). In order to replace via-holes used in 3D stacked chips, an asynchronous scheme is necessary as well as a source synchronous system. For asynchronous scheme was realized with single/double pulse encoding and a self-biased detector. For parallel data bus, the synchronous scheme was also developed. We call it Local Wireless Interconnection (LWI). It is applicable to parallel data transfer at arbitrary points of a chip. A LWI test chip with 12 channels has been designed and fabricated using a 0.18 $\mu$ m CMOS technology. Power dissipation was reduced to 0.95mW at 1Gbps. Bit error rate of  $10^{-10}$  was attained with relaxed alignment accuracy of 20 $\mu$ m.<sup>[5]</sup> (Fig.6) In the synchronous transmission scheme, the maximum bit rate of 2.3 Gbps was obtained by the same device and circuit techniques. These techniques will be also applicable to various type of interconnects such as chip-to-PCB or System-in-Package.

### 5.2 Standing-Wave Clock Distribution

Prof. Sasaki has developed new scheme for over 10GHz clock generation and distribution using inductor loaded and inductor coupled standing-wave oscillators. The proposed standing wave oscillator (SWO) has uniform-phase and almost uniform-amplitude and achieves clock distribution to

a whole chip area. It results in small latency, and low jitter and low skew.<sup>[6]</sup> By utilizing the inductor loaded SWO, a new mesh structure has been proposed. Mutual coupling of inductors placed at the end of TL, synchronizes the oscillation. The 12GHz operated test chip was prototyped in a 0.18 $\mu$ m CMOS technology. A jitter of 4.7ps peak-to-peak was achieved. The power consumption was 80mW at a supply voltage of 0.9V. As compared with the conventional structure, the proposed scheme reduces the area overhead. This technique is effective to 3-D integration.<sup>[7]</sup> (Fig.7)

### 5.3 CAM based parallel processing system

Prof. Mattaush and Kiode have developed CAM based image processing techniques.

#### [An associative memory architecture]

An associative memory for Nearest Euclidean Distance Search has been developed, which realizes for the first time fully-parallel minimum Euclidean-distance search. In this architecture we use a mixed digital-analog Euclidean distance calculation circuit with an analog squarer as key element and a fast analog winner search circuit for finding the nearest match. The architecture is verified by a 5.24 mm<sup>2</sup> test-chip design in 0.35 $\mu$ m CMOS technology, which searches 64 reference patterns in parallel in less than 140 nsec, and has a processing power equivalent to a 32-bit processor with 172 GOPS.<sup>[8]</sup> (Fig. 8)

#### [A learning model and application to handwritten character Recognition]

A learning model based on a short/long-term memory and an optimization algorithm for constantly adjusting the reference patterns, have been proposed. The major blocks of the system were implemented in an FPGA platform and tested with real data samples of handwritten and printed English characters. The simulation results showed an acceptable performance of classification and learning. In order to enhance the search speed in the classification block, we are planning to use a fully parallel associative memory implemented in LSI architecture, as the main classifier of the system via an ASIC design.<sup>[9]</sup>

### 5.4 Low Voltage Low noise Analog design Techniques

#### [Chopper amplifier and ring-VCO]

Dr. Yoshida has developed noise reduction techniques for CMOS analog and RF circuits operated at a low supply voltage below 1V. First, autozeroing and chopper stabilization techniques without floating analog switches were proposed. The amplifier test chip with a 0.18- $\mu$ m CMOS was measured at a 0.6-V supply, and achieved 89-nV/ $\sqrt{\text{Hz}}$  input referred noise (@100Hz).<sup>[10]</sup> Secondly, in RF frequency range, to improve a phase noise of voltage controlled oscillator (VCO), two 1/f-noise reduction techniques are described. The ring VCO test chip achieves 1-GHz oscillation, -68-dBc/Hz at 100-kHz offset, 710-uW power dissipation at 1-V power supply.

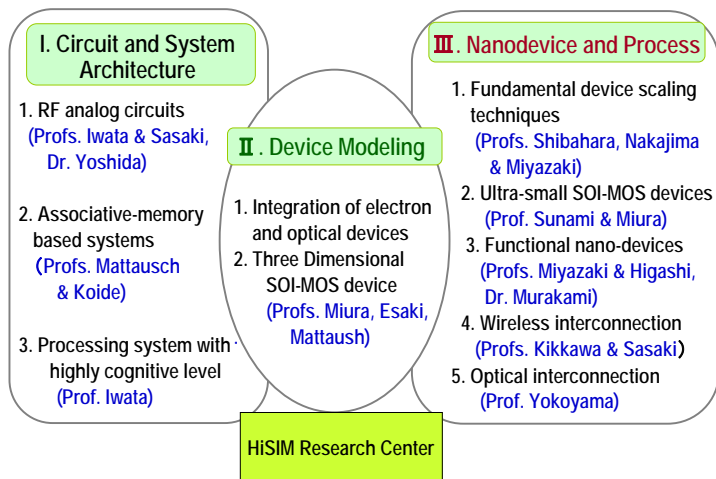


Fig. 1 Three Research Fields and Members of COE

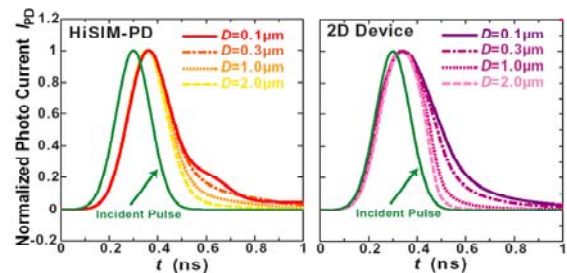
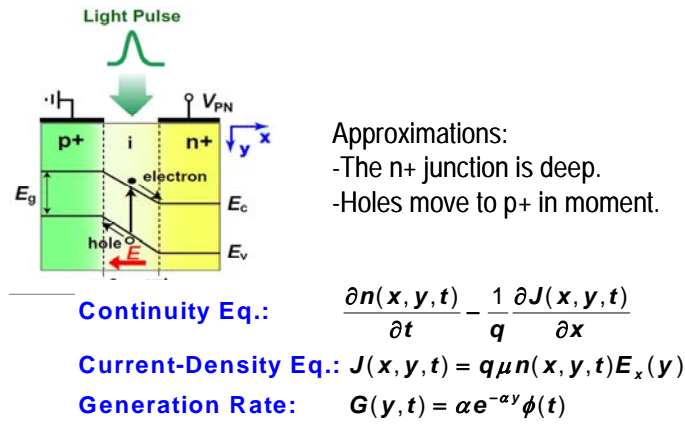


Fig. 4 Photodiode Model (HiSIM-PD)

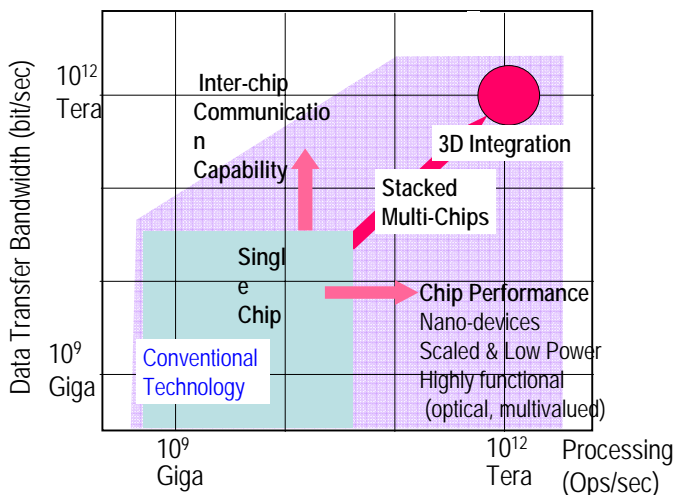


Fig. 2 Terabit Information Processing System

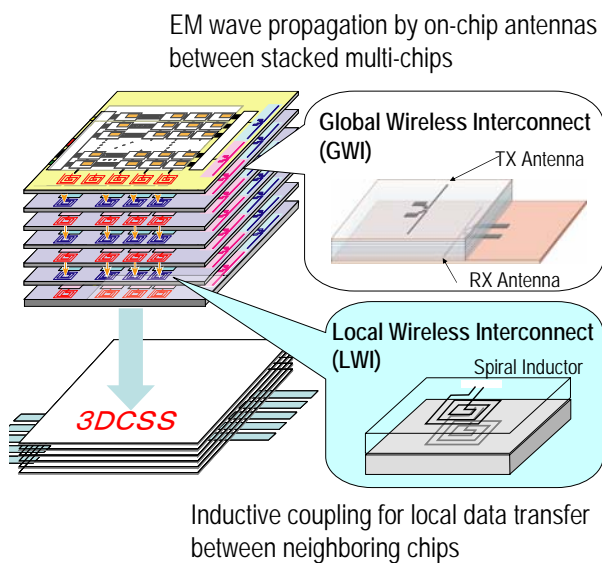
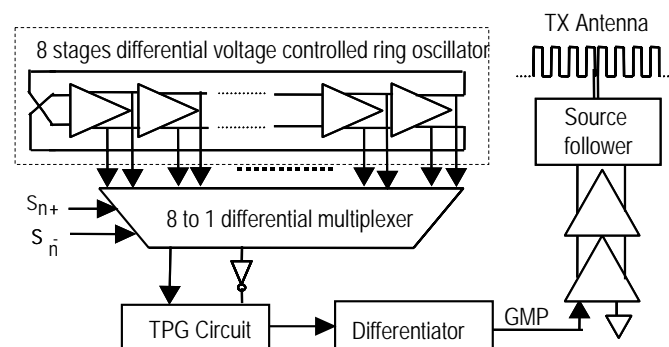
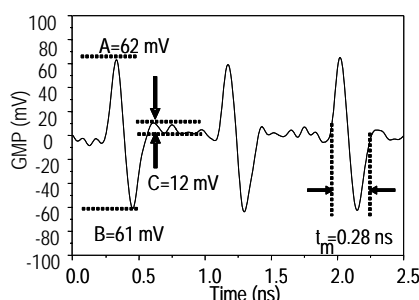


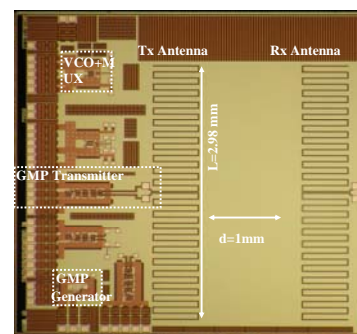
Fig. 3 Three-dimensional Custom Stack System (3DCSS) utilizing Wireless Interconnections



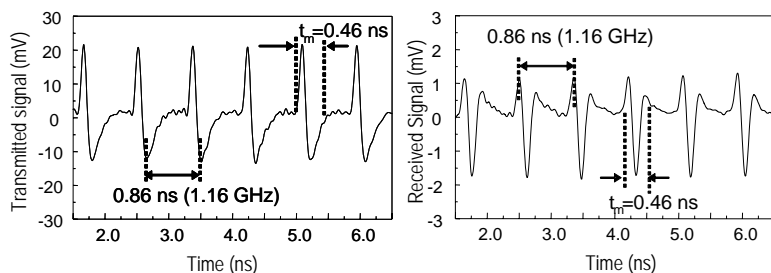
(a) Block diagram of Gaussian Monocycle Pulse Transmitter



(c) Generated GMP Signal



(b) Test Chip photo



(d) Measured Transmitted Signal

(e) Measured Received Signal

Fig. 5 Single-chip Gaussian Monocycle Pulse Transmitter

## [Measurement and analysis of substrate noise in scaled CMOS LSIs]

Prof. Iwata has developed advanced technologies for substrate noise measurement technologies. Substrate coupling effects in a 90nm CMOS technology were measured by the noise detection circuits integrated on a 1.2V standard-cell-based logic chip. Measurement results revealed frequency dependence of digital substrate coupling beyond 1GHz<sup>[11]</sup> Furthermore a real-time noise sensor macro has been developed on a 90 nm CMOS processor chip. It can measure single-events at 500MSPS real time sampling which continuously detects up to 100 noise events per second without disturbing processor operations.<sup>[12]</sup>

## 5.5 Architecture and implementation of prototype multi-object recognition system using 3DCSS

Prof. Iwata and COE member have proposed the 3-dimensional custom stack system (3DCSS) which use two kinds of wireless interconnections: inductive coupling local wireless interconnect (LWI) and antenna coupling global wireless interconnect (GWI)<sup>[1]</sup>. In the system, LWI is applied for 2D image data transfer between neighboring chips in parallel, and GWI is applied for communication of global system clocks, control signals and data-bus between all stacked chips.

To implement the multi-object detection/recognition system, the processing algorithm and system/chip architecture which are suitable to 3DCSS have to be developed. Although many kinds of algorithm have been reported in a field of human face recognition, the most of these were developed aiming at software realization and did not apply to LSI implementation, because of complex large-scale calculation and huge memory capacity.

Alignment accuracy of stacked chips is relaxed as low as about 10% of the inductor size. The distinguished feature of 3DCSS is to implement a customized system composed of various kinds of chips with multi functions and devices. Yield and Known Good Die (KGD) problems are also resolved by chip testing using wireless pads.

A higher resolution of pixels and customized functions are realized by 3DCSS. Dr. Ando adopted the Principal Component Analysis and the Eigenface method for realizing multi-object detection in a natural scene and recognition under significant image variations. Drs. Kameda, N. Sasaki and H. Ando have designed a prototype system using Flexible Printed Circuits technique. It is composed of wireless interconnected multi chips, early vision processor (VP3D), object detection/recognition (DR3D) and reference data storage (RM3D) (Fig. 9). Schematic and photo of 3DCSS prototype are shown in Fig. 10.

## 6. New MOS devices and process technologies

An overview of researches on devices and process technologies are shown in Fig. 11.

## 6.1 Work function tuning technology

The major subject of 3DCSS demands high-performance mixed-signal devices. The major targets in device technology are shallow junction formation and metal-gate workfunction tuning. These are standard development for CMOS logic application, in addition, helpful for improvement of RF characteristics. Low resistive shallow junction formation is indispensable to improve cut off frequency,  $f_T$  that is degraded by parasitic series resistance. Gate resistance reduction by replacing poly-Si gate with metal gate is effective for  $f_{MAX}$  improvement.

### [Shallow junction formation]

Prof. Shibahra has proposed PMLA (Partial Melt Laser Annealing) utilizing surface melt-process which provides high dopant activation and non-melt process for junction region to suppress increase in junction depth during annealing. By this method 10 nm junction with very low sheet resistance has been obtained.<sup>[13]</sup>(Fig.12)

### [Metal gate]

Pd2Si FUSI (Fully Silicided) gate process has been developed. Pd2Si is superior to conventional NiSi in terms of lower silicidation temperature and higher thermal stability. Workfunction tuning range with a predoping technique was compatible to that for NiSi. In addition, workfunction shift direction was opposite to NiSi.<sup>[14]</sup>

## 6.2 Atomic-layer deposition of gate dielectrics

Prof. Nakajima has developed future reliable gate dielectrics. The subject includes atomic layer deposition (ALD) of silicon nitride, ALD high- $k$  gate dielectrics, and plasma nitrided SiON gate nitride, etc.<sup>[15]</sup> A method to measure interface trap density and oxide trap density was developed. A method to measure interface trap density and oxide trap density separately for ultra-thin gate dielectrics were developed and applied it to plasma nitrided SiON gate nitride. The mechanism of dynamic bias temperature instability of gate dielectrics was investigated. (Fig.13)

Furthermore Atomic-layer-deposited Si-nitride/SiO<sub>2</sub> gate dielectrics were studied to apply to future scaled DRAM. Atomic layer deposition technique of HfO<sub>2</sub> gate dielectric was also developed and applied to MOSFETs.

## 6.3 Beam Channel Transistor

Prof. Sunami proposed the new 3-D structure of Beam Channel Transistor (BCT) to obtain high drivability with a small area and developed process technologies by fabricating the BCTs of 1.5- $\mu\text{m}$  beam height and 2.0 $\mu\text{m}$  gate length and of 1.0- $\mu\text{m}$  beam height and 0.2 $\mu\text{m}$  gate length. Main achievements in the process technologies are as follows.<sup>[16]</sup>

- 1) Aspect ratio of greater than 50 was obtained for (110) Si beam formation.
- 2) Selective oxide coating of Si gate process was developed for conformal gate formation.
- 3) Preliminary plasma doping process was developed for uniform doping to tall vertical Si side-wall.

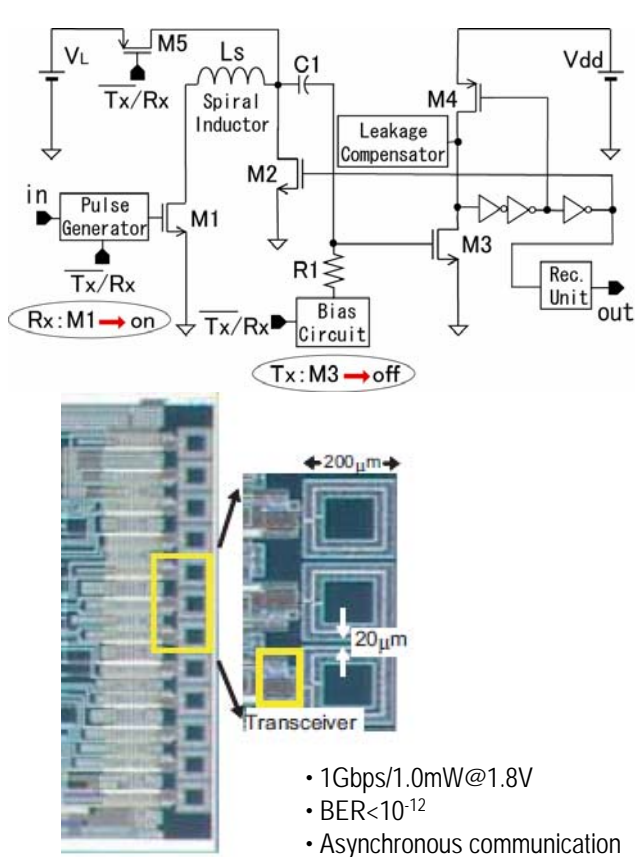


Fig. 6 LWI Transceiver circuit and its test chip

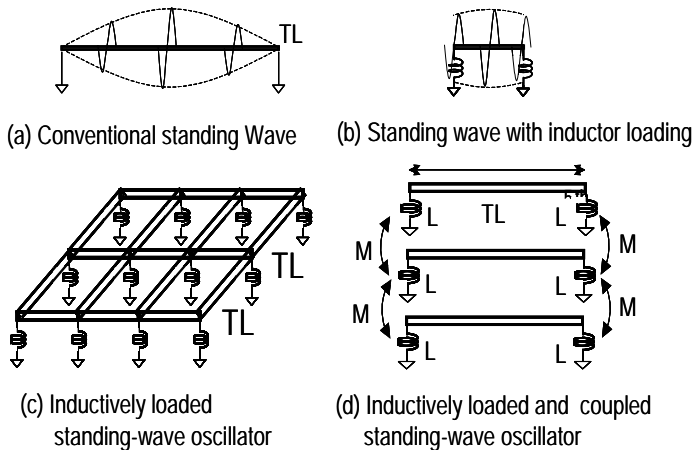


Fig. 7 Over 10GHz clock generation and distribution using L loaded standing wave oscillator

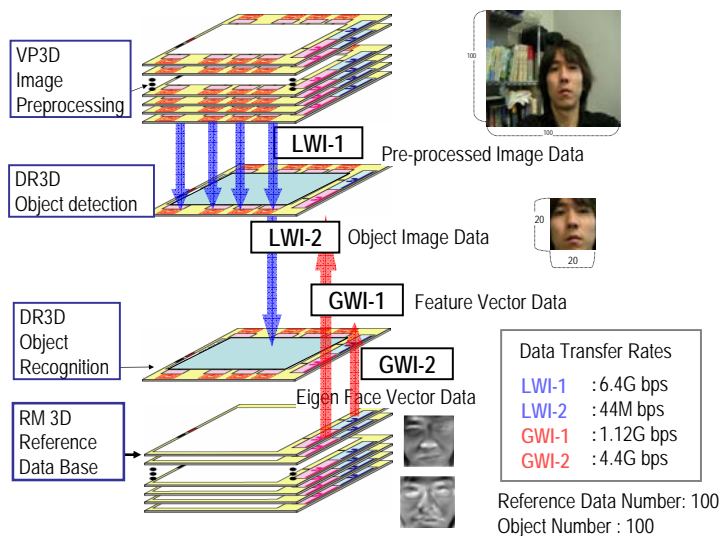
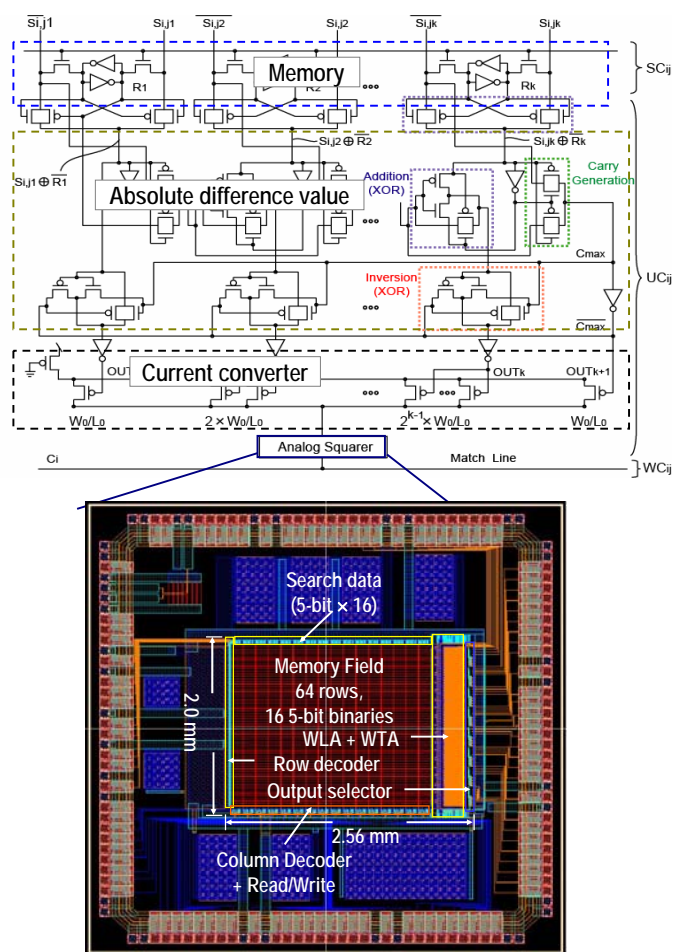


Fig. 9 Multi-Object Detection/Recognition system using 3DCSS



Designed test chip in 0.35um CMOS Technology.

Fig.8 Associative Memory for Nearest Euclidean Distance Search

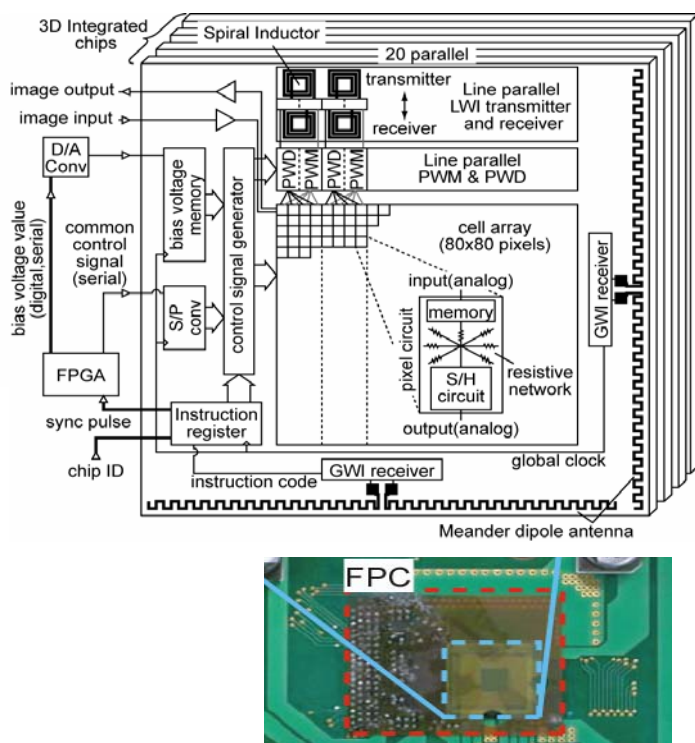


Fig.10 Prototype 3DCSS using FPC

- 4) A guiding principle for Ni-silicidation of tall SI beam was proposed for precise control of source/drain formation.
- 5) An independently controllable triple gate beam channel transistor was successfully developed. (Fig.14)

## 7. Integrated Optical devices

Prof. Yokoyama has studied the optical interconnection in LSI, in order to overcome the speed limit of the metal interconnection. The compact ring-resonator optical switches using electro-optic material which is integrated on the top layer in the LSI was proposed. The operation voltage is calculated to be less than 17 V depending on the core material. The operation frequency is 66GHz for the ring radius of 12  $\mu\text{m}$ .<sup>[17]</sup>

An operation of Mach-Zehnder modulator which is integrated on Si by using (Ba,Sr)TiO<sub>3</sub> film, has been obtained for the first time. The modulation efficiency of ~10% is obtained for the sputtered (Ba,Sr)TiO<sub>3</sub> film, but it will be improved by the optimum device design and material improvement.<sup>[18]</sup>

Furthermore, a ring-resonator optical switch using magneto-optic material has been proposed. The merit of this device is a low operation voltage less than 1V. Recently, we have succeeded in observation of the Faraday effect of the magneto-optic material Bi<sub>3</sub>Fe<sub>3</sub>O<sub>12</sub>. (Fig.15)

## 8. Characterization of Charged States of Si- Quantum Dots for Multi-valued Memories

To achieve multi-valued memory operations at room temperature, a precise control in discrete charged states in Si quantum dots (Si-QDs) is a key issue. (Fig. 16)

Prof. Miyazaki and Higashi and Dr. Murakami have focused on the control of charged states by impurity doping and also studied multiple step charging and discharging in the Si-QDs floating gate.

Charged states of individual Si-QD can be characterized by an AFM Kelvin probe technique which enables to detect the surface potential change caused even by single electron injection or extraction. The surface potential changes were characterized for undoped, P-doped and B-doped Si-QDs.

Multiple step electron injection to the Si-QDs floating gate has been confirmed by temporal drain current changes.

By applying pulsed gate bias, the progress in charging to or discharging from the Si-QDs floating gate has been studied. The drain currents just after positive and negative gate pulses are evaluated as functions of pulse height. In both electron charging and discharging,<sup>[19]</sup> (Fig. 17)

## 9. Future Project for Semiconductor and Bio Integration

Based on the achievements of the COE program, we proposed the innovation project for “semiconductor and biotechnology integration”, in cooperation with the members of bio-science in Hiroshima University and ELPIDA memory Corp. The proposal was accepted in July, 2006. This project is aiming at fusion of bio- and silicon-technologies and establishment of an innovation center in

- (1) bio-sensing systems for detecting bacteria and allergens,
- (2) tera-bit memories using a new principle and materials,
- and (3) human brain like information processing systems which consist of sensors and memories.

A new research institute for integration of Life science and Nano-electronics will be established, where research collaboration on nano-bio-sensor fusion, next generation memory technologies will be conducted.

## 10. Conclusions

The COE program has established extensive collaboration in the research fields of circuits and devices, and developed the innovative 3D integration technology utilizing wireless interconnections and the related device and design techniques. The achievement will lead us to the future research in nano-bio fusion technologies.

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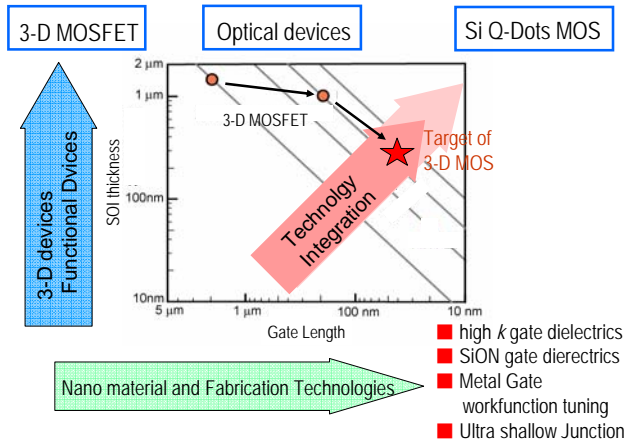
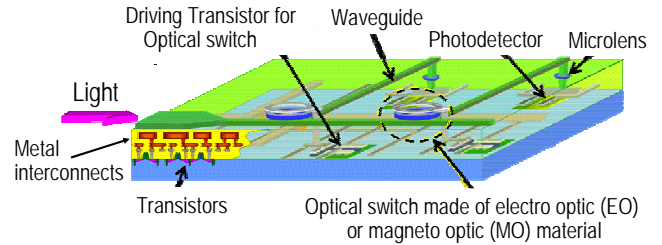
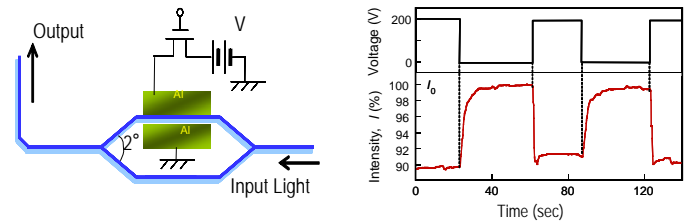


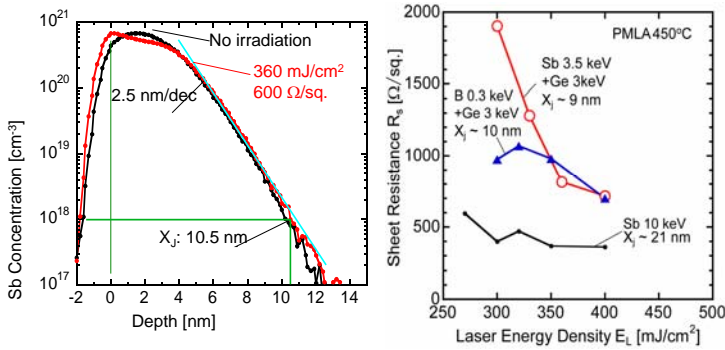
Fig. 11 Overview of nano-device and process technologies



(a) Schematic View of Optical Interconnected LSI



(c) Mach-Zehnder Modulator and modulated Intensity



World leading shallow junction formation maintaining low sheet resistance by PMLA (Partial Melt Laser Annealing)

Fig. 12 10 nm Junction Formation with Sb and B

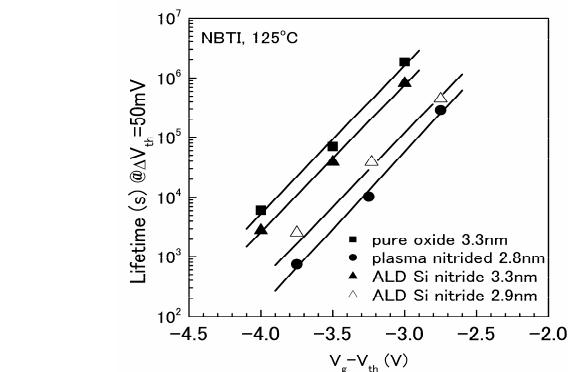


Fig. 13 Lifetime of ALD Si Nitride gate device as a function of  $V_g - V_{th}$

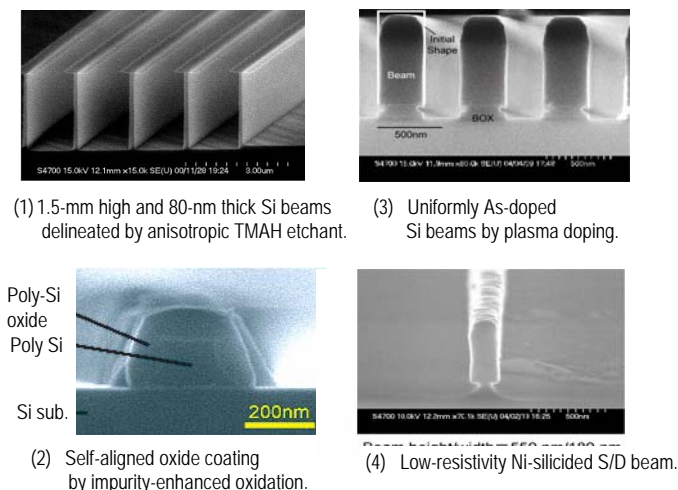
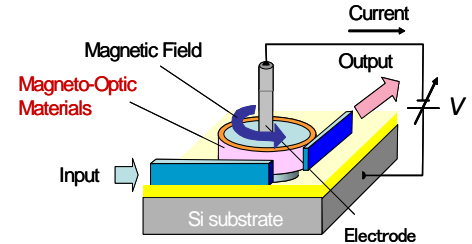
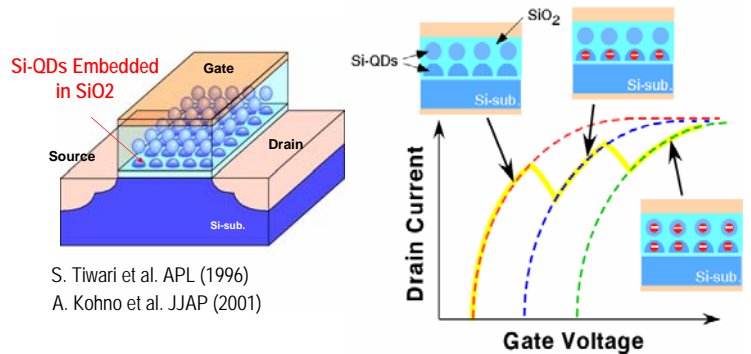


Fig. 14 Results of process for Beam channel Transistor



(c) Ring Optical SW using MO materials

Fig. 15 Optically interconnected LSI and its components



S. Tiwari et al. APL (1996)  
A. Kohno et al. JJAP (2001)

Electrical Interaction & Coupling among Electronic States in Neighboring QDs

Fig. 16 Si-QDs Floating-Gate MOS Memories Multi-valued & Low-Voltage Operations at Room Temp.

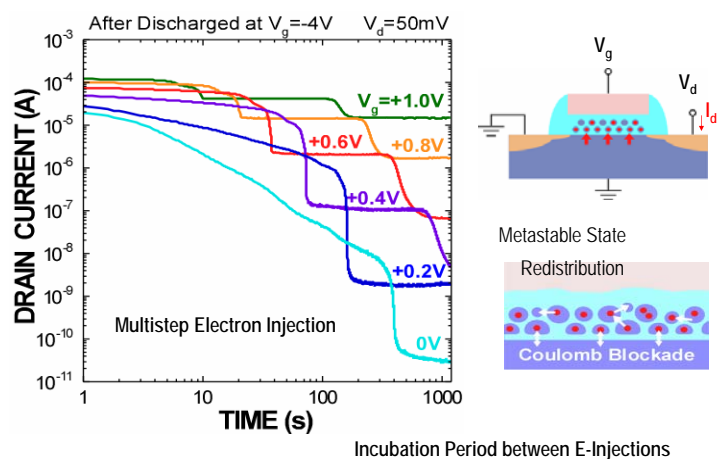


Fig. 17 Transient  $I_d$  Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate