21st Century COE, Hiroshima University
Nanoelectronics for
Tera-bit Information Processing

Summary of the 21st COE Program on Nanoelectronics for Tera-bit Information Processing

Atsushi Iwata, COE Leader
Jan. 29, 2007

Outline

1. Concept and target of the COE
2. Research fields and Members
3. Modeling -*HiSIM*
4. Circuits and System -*3DCSS*
5. Devices and Process
6. Future project for Semi-Bio integration
7. Conclusion

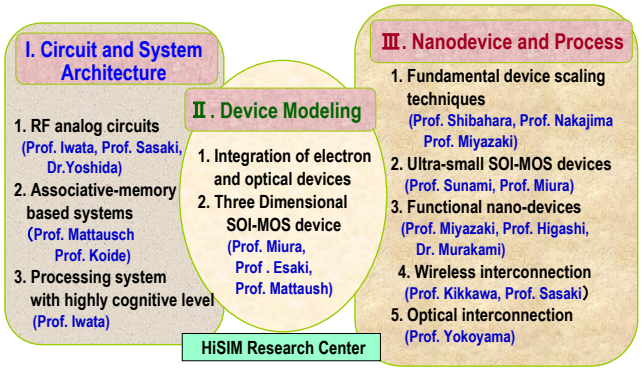
Concept and Target of the COE

Concept is to realize
Collaborative research in these 3 fields of
(1) circuit design and system architecture,
(2) device modeling, (3) nano-devices and processing.
RF operated device structure predicted by physical modeling.

Targets is to develop innovative tech. for implementing hyper brains with tera-bit processing capability.
That is 3-D integration utilizing wireless Interconnects, and related nano-device, materials and processing tech.

Objective in education is to bring up highly-capable human resources who become leaders.

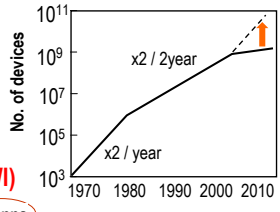
Three Core Research Fields and Members



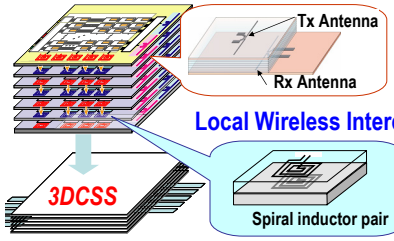
started in May 2005
for international standard MOS device Model

3D Integration using Wireless Interconnects

To overcome the Moore's law by utilizing 3D integration, **new interconnection tech.** is required.



Global Wireless Interconnect (GWI)



EM wave propagation through stacked multi-chips for Global clocks and data

Local Wireless Interconnect (LWI)

Inductive coupling between adjacent chips for local data transfer

Presented at ISSCC2005

HiSIM MOS Model

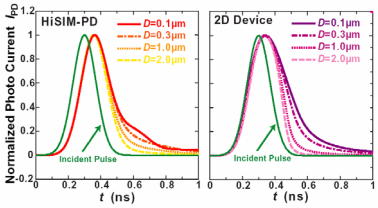
HiSIM model described by the surface potential based on drift and diffusion.
HiSIM2 including Non-Quasi-Static effects realizes sufficient accuracy in noise and distortion at GHz RF circuit operation.

Model	Year 96 98 00 02 04 06	Nr. of model parameter	Physics based	Accuracy, reliability
BSIM (UC Berkeley)	Ver.Ⅲ Ver.Ⅳ	300	×	×
Model 11 (Philips) SP2000 (U. Penn. St.) Surface Potential (anal.)	PSP		○	△
HiSIM (Hiroshima U.) Surface Potential(exact)	Ver. Ⅰ Ver. Ⅱ	75	○	○

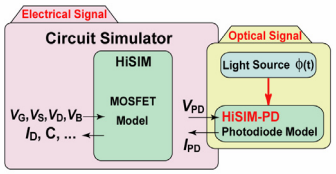
Compact Model Council selected the next MOS model by the end of 2005.
HiSIM was selected a promising candidate of 1st stage in July 2004,
PSP was selected the standard MOS model at the end of 2005.
Study on other devices: SOI device, DMOS is continued.

Modeling of Lateral Photodiode

HiSIM-PD considering the transient carrier generation explicitly in the solution of the continuity equation



Electric field distribution along depth direction is found to cause a tail in the photo current.



HiSIM-PD model can be installed into circuit simulator and enables to simulate opto-electronic system.

Presented at IEDM2006

System and Circuit Architecture

1. Wireless Interconnections

- GWI: UWB transceiver with on-chip antenna
- LWI: Asynchronous and synchronous scheme
- Standing wave oscillator using inductors
- Low noise & low voltage analog circuits

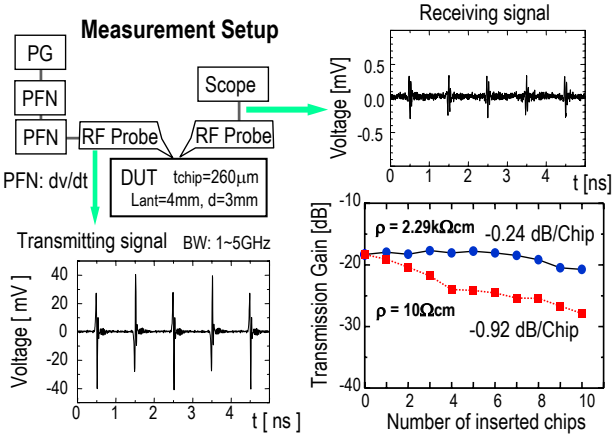
2. Memory based Parallel Processing

- Associative memory: **Eucridean dis. cal.** & learning
- Learning model & application to handwritten character recog.

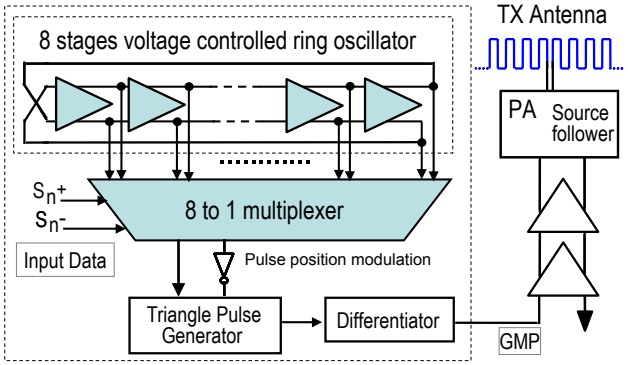
3. Three Dimensional Integration using GWI & LWI

- 3-Dimentional Custom stack system: 3DCSS
- Multi-object recognition prototype consists of 3 chips
  VP3D, OR3D, RM3D and FPC

Transmission of Gaussian Monocycle Pulses

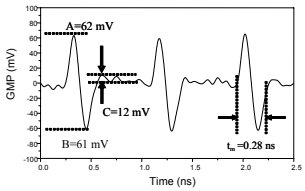


A Gaussian Monocycle Pulse Transmitter Circuit For IR-UWB system

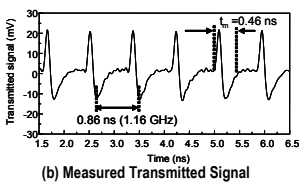


Presented at Symp. on VLSI Circuits 2006

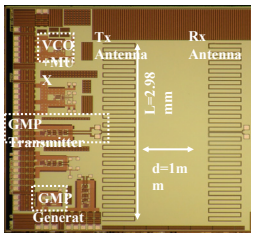
Measurement Results of Gaussian Monocycle Pulse Transmitter using 0.18um CMOS

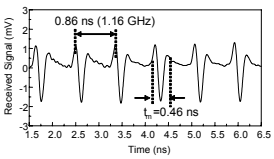


(a) Generated GMP waveform



(b) Measured Transmitted Signal

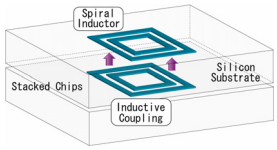




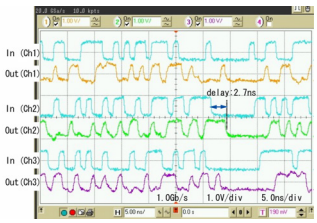
(c) Measured Received Signal

Presented at Symp. on VLSI Circuits 2006

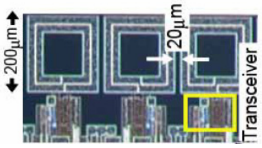
Spiral-inductor based wireless chip-interconnect



(a) Spiral inductor pair on stacked Chips



(c) Transmitted data and received waveforms

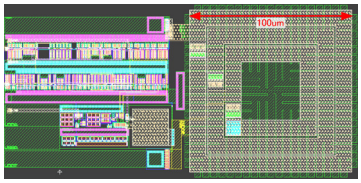


(b) Photomicrograph of test chip

- 1Gbps/1.0mW@1.8V
- BER<10^{-12}
- Asynchronous communication

Symp. on VLSI Circuits, pp.348-351, June 2005.

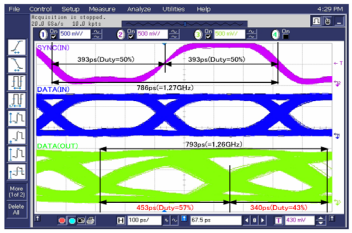
LWI Transceiver using 0.18 um CMOS



Layout

Inductor

ESD is not required



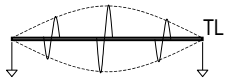
Clock using both edge

Transmitting data

2.3Gbps

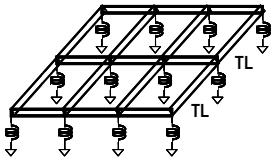
Receiving eye pattern

Over 10GHz clock generation and distribution using L loaded standing wave oscillator

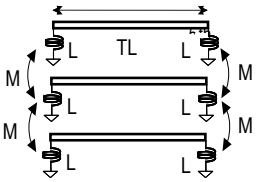


(a) Conventional standing wave

(b) Standing wave with inductor loading



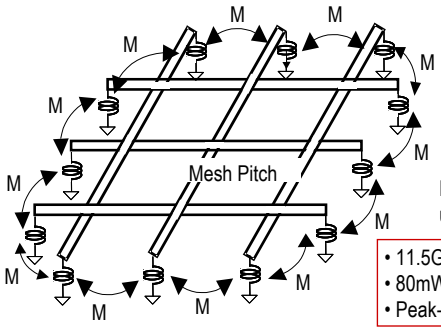
(c) Inductively loaded standing wave oscillator mesh



(d) Inductively loaded and coupled standing-wave oscillators

Presented at Symp. on VLSI Circuits 2006

Over 10GHz clock generation and distribution using L loaded standing wave oscillator



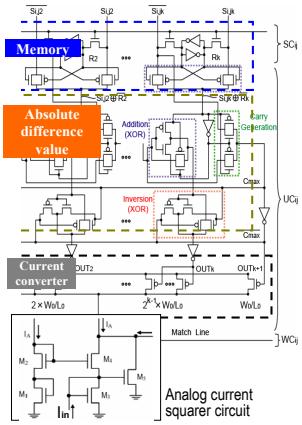
By the measurement using C coupling probe

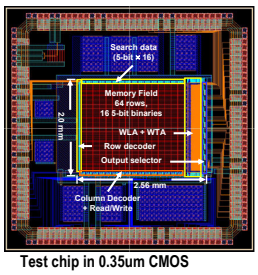
- 11.5GHz, 0.6Vpp Oscillation
- 80mW@0.9V (5x5 mesh)
- Peak-peak Jitter 4.7ps

To be presented at ISSCC 2007

the scheme reduces the area overhead. and effective to clock distribution for 3-D system.

Associative Memory for Nearest Euclidean Distance Search



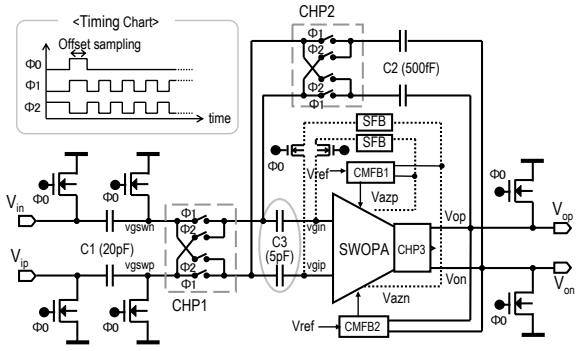


Test chip in 0.35um CMOS

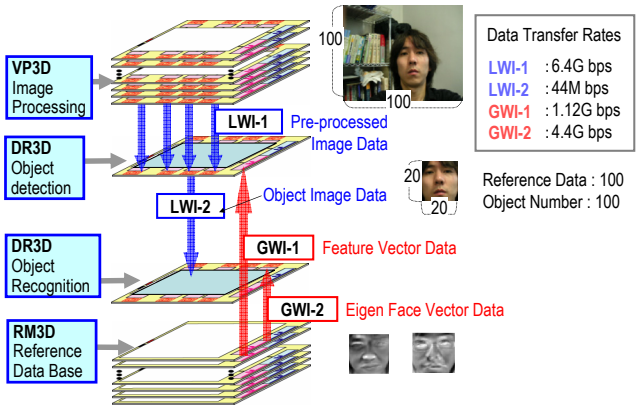
Reference Patterns	64 Patterns (16 binaries each 5-bit long)
Design Area	5.12 mm² (2.56mm x 2mm)
Nearest Match Times (simulation)	< 140 nsec
Power Dissipation (simulation)	< 220 mW
Chip size	4.9 mm × 4.9 mm

Low Voltage Chopper Amplifier operated at 0.6V Supply

Noise reduction techniques AutoZeroing and Chopper stabilization using grounded switches, and bias



Multi-Object Detection/Recognition System using 3DCSS



Data Transfer Rates

LWI-1 : 6.4G bps

LWI-2 : 44M bps

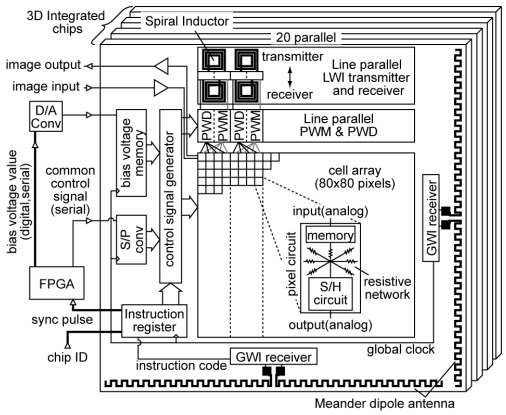
GWI-1 : 1.12G bps

GWI-2 : 4.4G bps

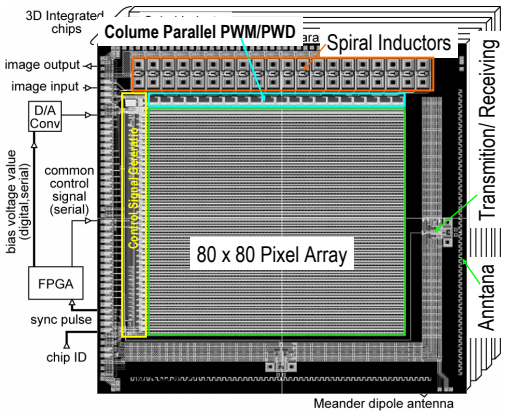
Reference Data : 100

Object Number : 100

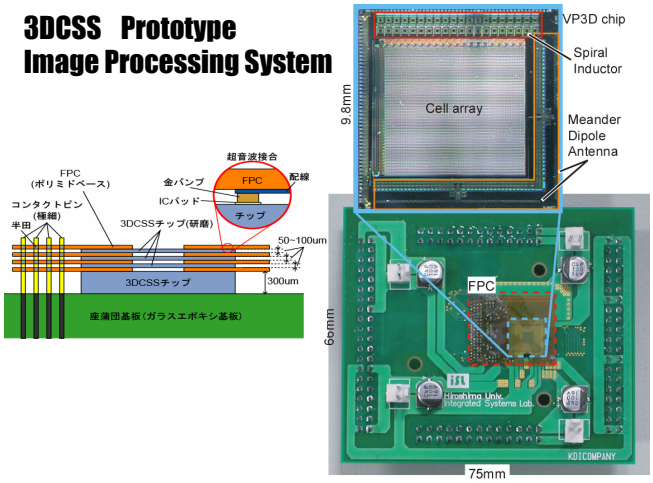
Vision Proc. Chip for 3D integration (VP3D)



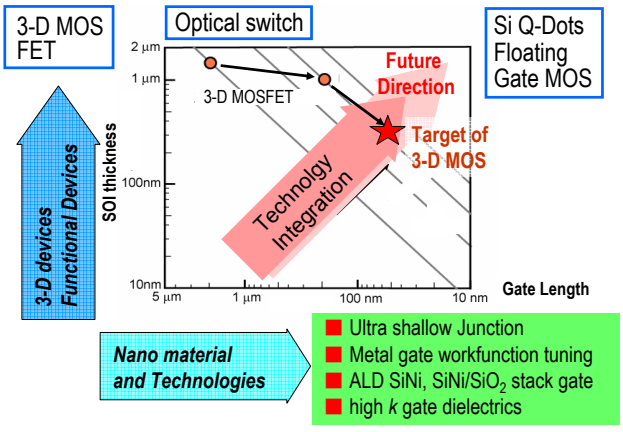
Vision Proc. Chip for 3D integration (VP3D)



3DCSS Prototype Image Processing System



Overview of nano-device and process technologies



Process Tech. for scaled & 3-D MOS devices

1. Ultra-shallow junction and gate workfunction tuning

- **10 nm Junction formation with Sb and B** by PMLA (Partial Melt Laser Annealing)
- **Work function tuning for NiSi Gate MOS FETs**
  Solution: Sb pre-doping before silicidation
  Study on new metal gate material: Pd_2Si (FUSI)

2. Highly reliable High-k gate dielectrics using ALD

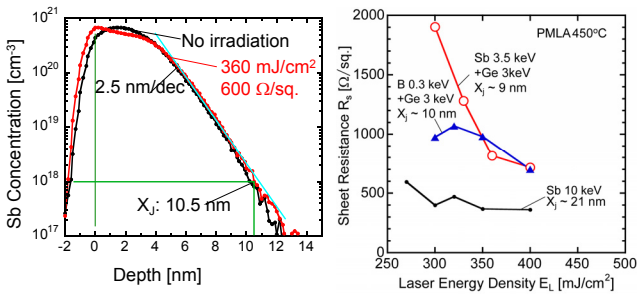
- Si-nitride/SiO2 stack gate dielectrics for scaled DRAMs
- New high-k gate dielectrics - HfO_2

3. 3-D MOS Devices: Beam Channel Transistor with
high current driving capability with small chip area.

- Structure and processing

10 nm Junction Formation with Sb and B

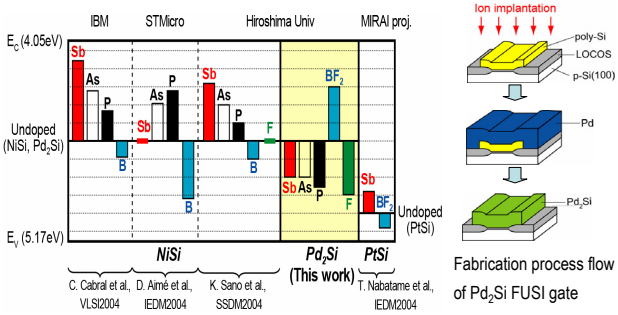
World leading shallow junction formation maintaining low sheet resistance by PMLA (Partial Melt Laser Annealing)



Ext. Abst. IWJT, 2005, pp. 53-54. Invited
IEEE Trans. Electron Devices, **53** pp. 1059-1064, 2006

New Metal Gate Material: Pd_2Si FUSI

Pd_2Si FUSI (Fully Silicided): lower silicidation temperature and higher thermal stability than conventional NiSi FUSI



Fabrication process flow of Pd_2Si FUSI gate

Workfunction tuning range: compatible to NiSi FUSI

Ext. Abst. Int. Conf. 2006 SSDM, pp. 218-219.

Reliable gate dielectrics using ALD

The research includes
1. ALD of Si nitride
2. ALD high–*k* gate dielectrics
3. plasma nitrided SiON gate

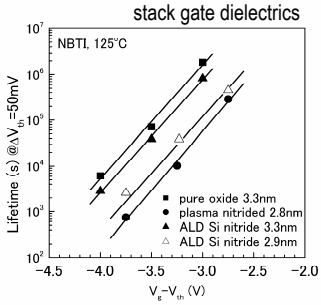
A method to measure the density of interface trap and oxide trap for ultra-thin gate dielectrics was developed.

ALD Si-nitride/SiO2 stack gate dielectrics were studied to apply to DRAMs.

Device life time was confirmed as the same order of the pure Si nitride.

Device lifetime as a function of V_g- V_{th}

ALD Si nitride/SiO2 stack gate dielectrics



EDL 26, 538 (2005)

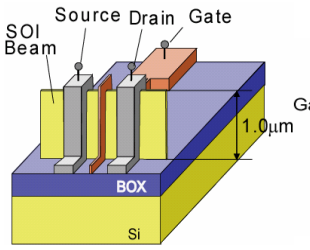
Technologies to realize BCT target-A and -B

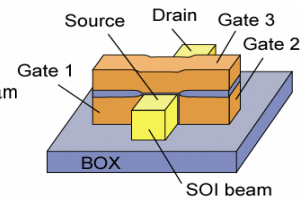
Tall Si beam structure

Technologies required
(1) Tall beam formation
(2) Conformal gate formation
(3) Uniform impurity doping
(4) Wrapped S/D contact

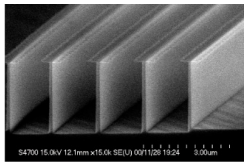
Triple gate structure

Technology required:
Highly self-aligned process

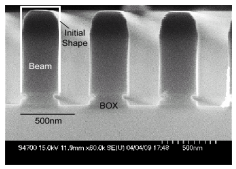




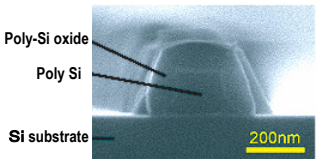
Results of process development



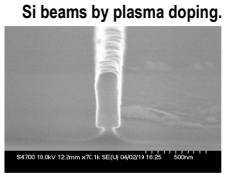
(1) 1.5-μm high and 80-nm thick Si beams delineated by anisotropic TMAH etchant.



(3) Uniformly As-doped Si beams by plasma doping.



(2) Self-aligned oxide coating by impurity-enhanced oxidation.



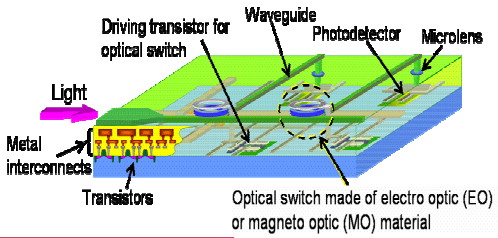
Beam height/width=550 nm/180 nm

(4) Low-resistivity Ni-silicided S/D beam.

Results of fabrication process for BCT

1. Aspect ratio of greater than 50 is obtained for (110) Si beam formation.
2. Selective oxide coating of Si gate process is developed for conformal gate formation.
3. Preliminary plasma doping process is developed for uniform doping to tall vertical Si side-wall.
4. A guiding principle for Ni-silicidation of tall Si beam is proposed for precise control of source/drain formation.
5. An independently controllable triple gate beam channel transistor is successfully developed.

Optically Interconnected LSI

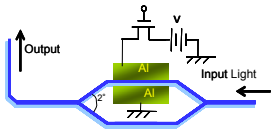


Jpn. J. Appl. Phys. 45, No. 4B, p. 3488, 2006

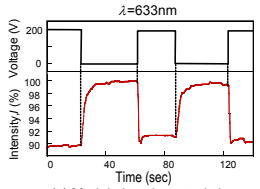
Ring resonator optical switch using electro-optic (EO) material
Switching speed 66 GHz operation at <20V (Simulated)

Formation of EO material **$(Ba,Sr)TiO_3$** at low temperatures (≤550 °C) by sputtering and spin-coat

Monolithic Mach-Zehnder interferrometric modulator



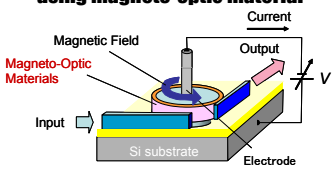
(a) Structure using (Ba,Sr)TiO3 film



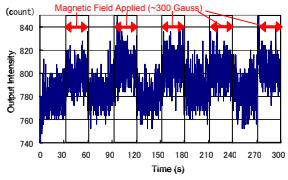
(a) Modulation characteristics

Appl. Phys. Lett. **88**, No. 16, 161107 (2006).

Ring resonator optical switch using magneto-optic material



(a) Structure

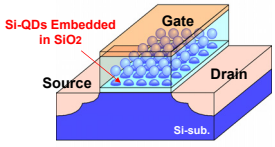


(a) Modulation characteristics

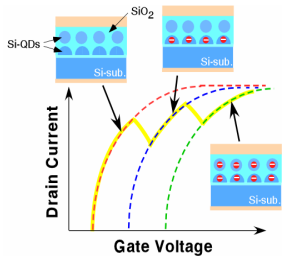
Latest experimental result (unpublished)
~2% modulation achieved for $Bi_3Fe_5O_{12}$ film sputtered at RT.

Si-QDs Floating-Gate MOS Memories Multivalued & Low-Voltage Operations at Room Temp.

Floating Gate Application of Si Quantum Dots



S. Tiwari et al. APL (1996)
A. Kohno et al. JJAP (2001)

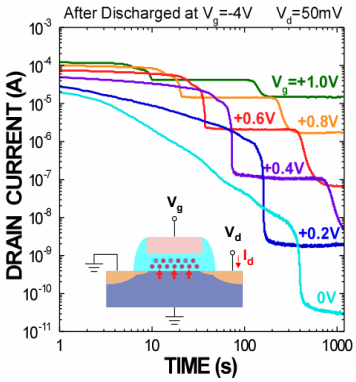


☆**Control of Discrete Charged States in Si-QDs**

⇩

Electrical Interaction & Coupling among Electronic States in Neighboring QDs

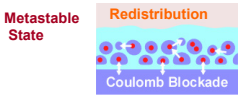
Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate



Multiple step electron injection to the Si-QDs floating gate device has been confirmed by the temporal drain current changes.

Increase in Id due to electron emission is observed by Vg switching in a metastable state.

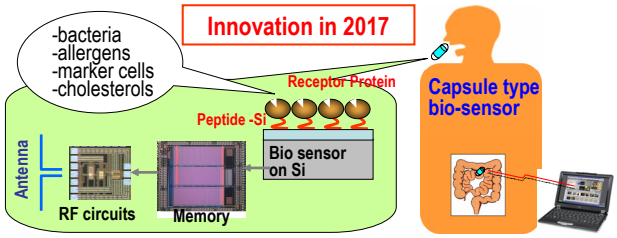
During each metastable state, electrons injectedare likely to be redistributed.



Innovation Project for Semi-Bio Integration

Based on the achievement of the COE program, we have started the project for **semiconductor and biotechnology integration** in cooperation with ELPIDA memory Corp.

Target of the project is **capsule type bio-sensor systems** with multi-item / sensitive bio sensing, memory and wireless I/F which brings **ubiquitous medical examinations**.



Conclusions

The COE has established intensive collaboration in the research fields of circuits/system, modeling and device/process.

The innovative 3D integration technology utilizing wireless interconnections and the related device and design techniques have been developed.

The achievement will lead us to the future research in **nano-bio fusion technologies**.