Reconfigurable Parallel Image Processing System Using Three-Dimensional LSI

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Outline

1. Introduction
2. 3D Integration Technology
3. Fabrication of 3D LSI and New Applications
4. Reconfigurable Parallel Image Processing System
5. Summary

Prospective Market for Future Semiconductor Technology

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Diverse and Expanded Market

Qualitative Change of Semiconductor Technology

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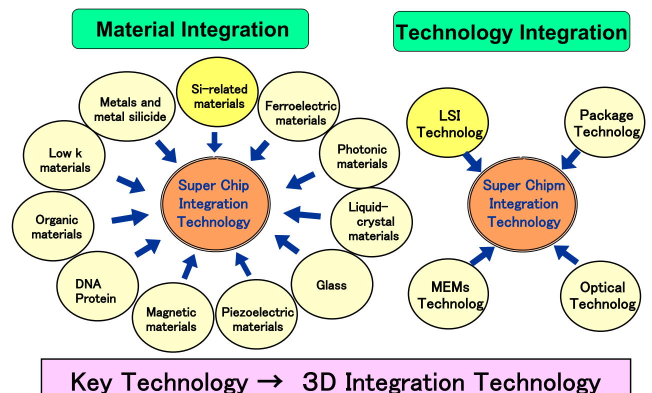
Technology Integration

Key Technology → I T
Nano Technology
Bio Technology
Robotics Technology

New System Integration Technology

Super Chip Integration (SCI)



Key Technology → 3D Integration Technology

Research Projects in Koyanagi's Laboratory

1. Ultra small semiconductor device and process
2. New functional memory devices
3. Low power circuits
4. Bio-inspired circuits
5. Three-dimensional integration technology
6. Optical interconnection
7. Bio-chip and bio-electronic system
8. Artificial retina chip and brain-type computer
9. Information processing system with 3D structure
10. Parallel processing computer system

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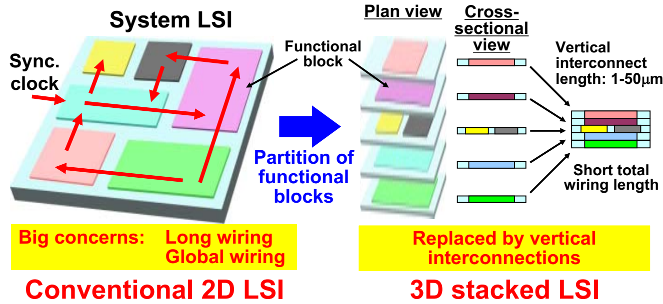
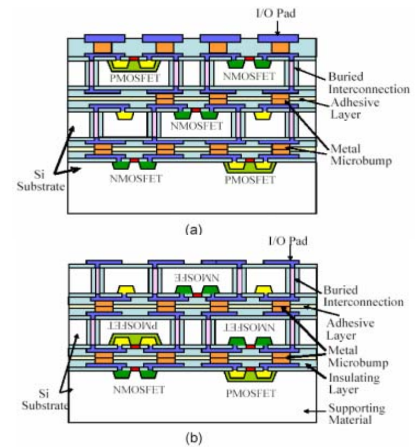
Advantages of 3D Integration Technology

1. Short interconnect length
2. High packing density
3. High-speed operation
4. Low power consumption
5. Parallel processing
6. New functionality
7. New applications



Cross-Sectional Structure of 3D LSI

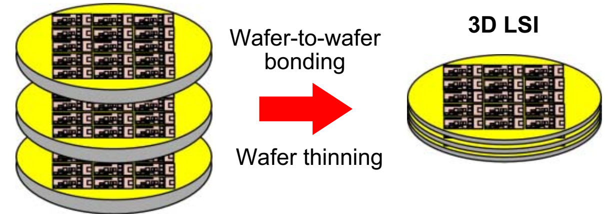


Outline

1. Background
2. 3D Integration Technology Based on Wafer-to-Wafer Bonding
3. 3D Integration Technology Based on Chip-to-Wafer Bonding
   - Super Chip Integration -
4. Fabrication and Evaluation of 3D LSI Test Chips
5. New Applications for 3D LSI
6. Summary

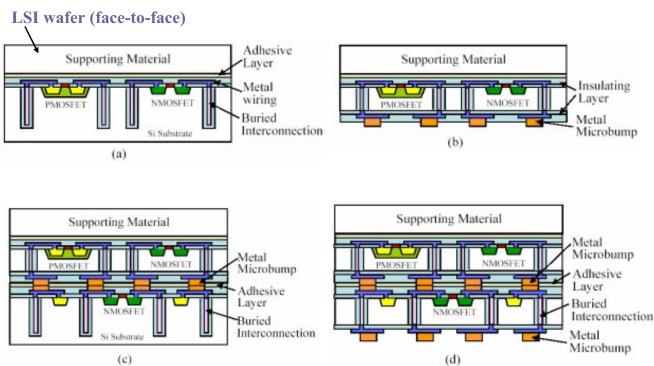
3D Technology Based on Wafer-to-Wafer Bonding in Tohoku University

Completed LSI wafers with vertical interconnection

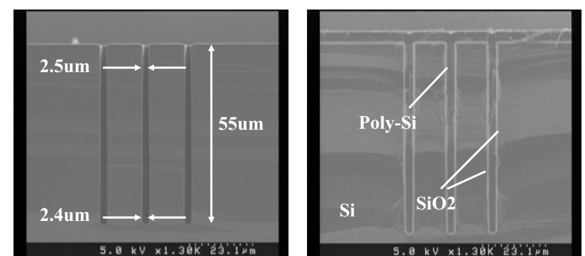


First Proposal of Wafer-to-Wafer Bonding Technique (1989)

Fabrication Sequence of 3D LSI

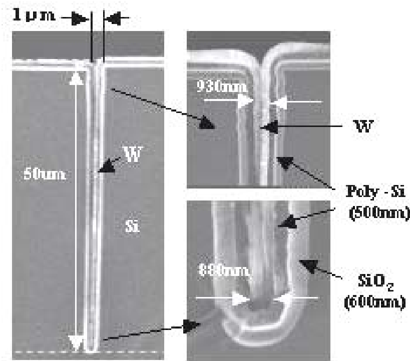


SEM Cross Section of Poly-Si Buried Interconnection

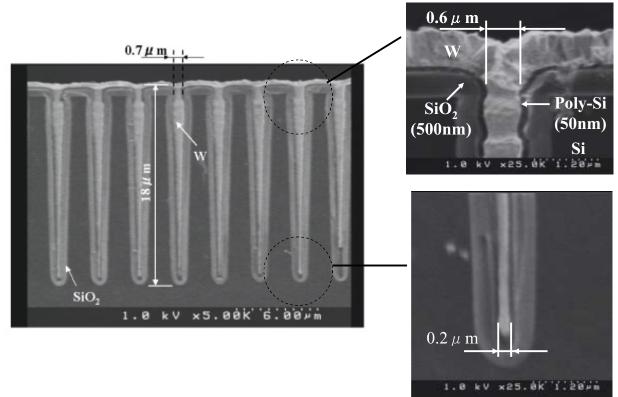


(a) Si deep trench etching (b) Filling with Poly-Si

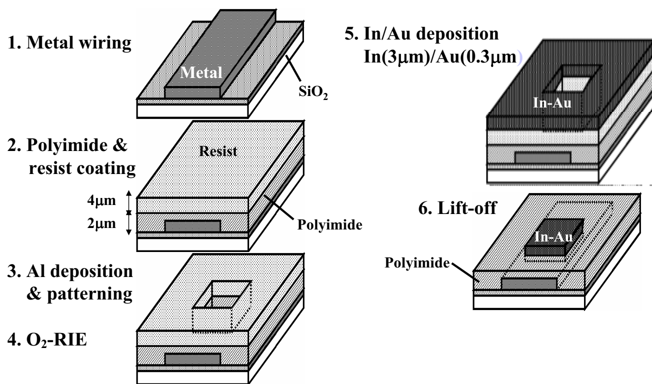
SEM Cross Section of Tungsten Buried Interconnection



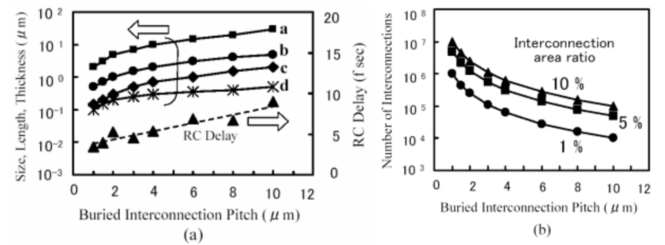
SEM Cross Section of Tungsten Buried Interconnection with Smaller Diameter



Fabrication Sequence of In/Au Microbump Using New Planarized Lift-off Method

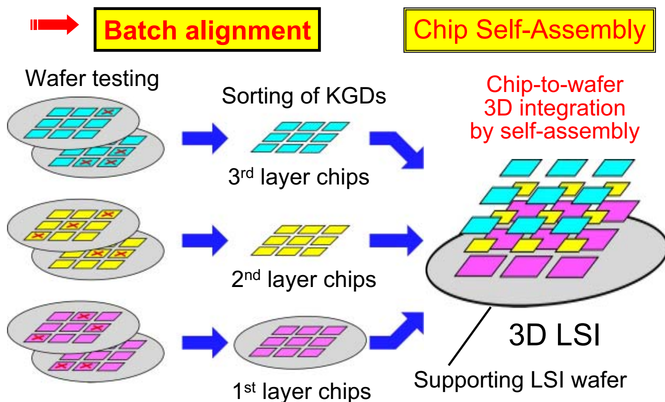


Scaling Capability of Buried Interconnection

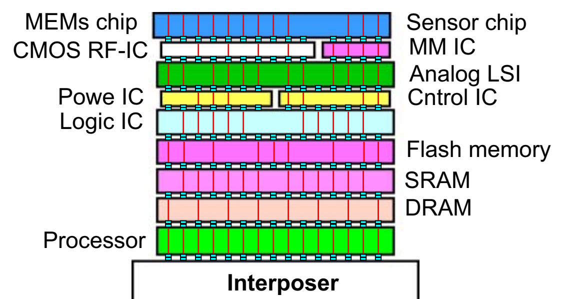


a: buried interconnection length, b: microbump size,
c: buried interconnection diameter, d: insulator thickness.

3D Technology Based on Chip-to-Wafer Bonding in Tohoku University : Super-Chip Integration



Configuration of Super-Chip



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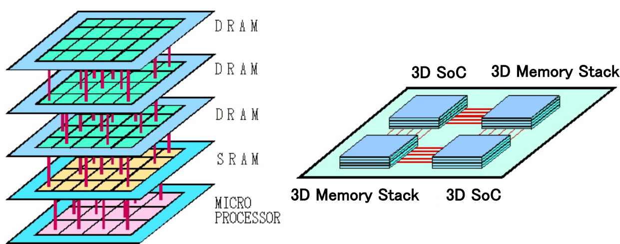
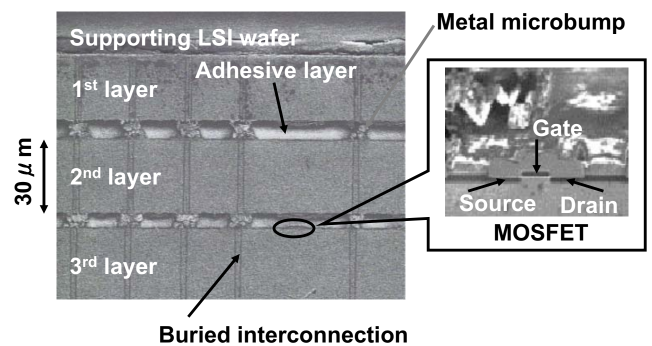
3D LST Test Chips Fabricated in Tohoku University

- 3-layer stacked image sensor chip (IEDM, 1999)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked memory chip (IEDM, 2000)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked artificial retina chip (ISSCC, 2001)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked microprocessor chip (Cool Chips, 2002)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 10-layer stacked memory chip (IEDM, 2005)
  Chip-to-wafer bonding (Self assembly, Buried interconnection)

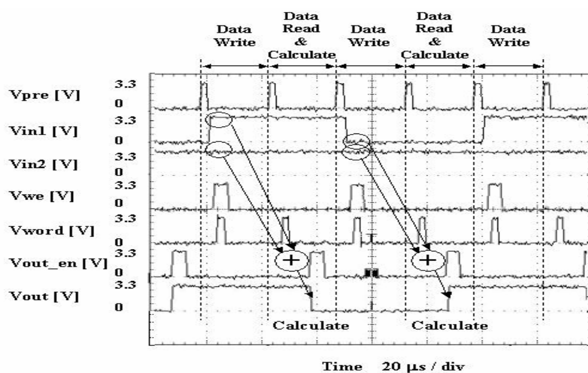
3D Computer Chip and 3D Multi-chip Module



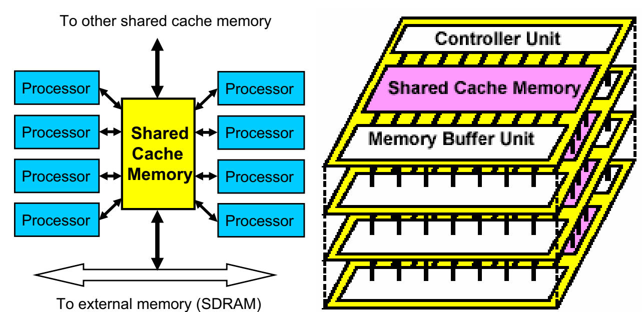
SEM Cross-Sectional View of 3D Microprocessor Chip Fabricated by Wafer-to-Wafer Bonding



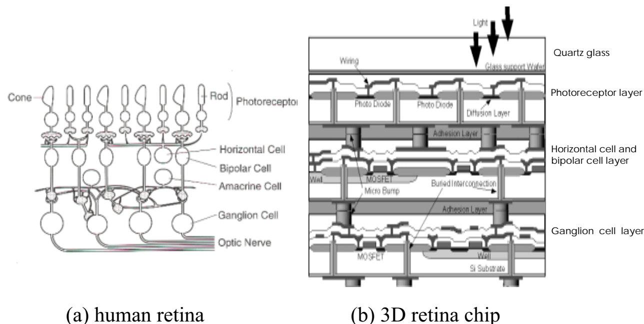
Measured Waveforms of 3D Microprocessor Test Chip (SRAM layer: 3.3V, Processor layer: 2.5V)



Shared Cache Memory with 3D Structure

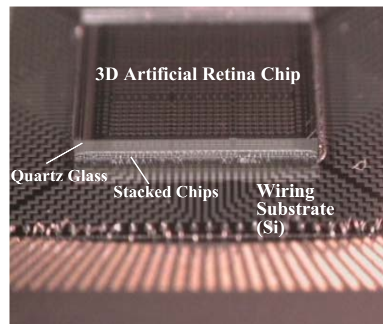


Cross-Sectional Structures of Human Retina and 3D Artificial Retina Chip

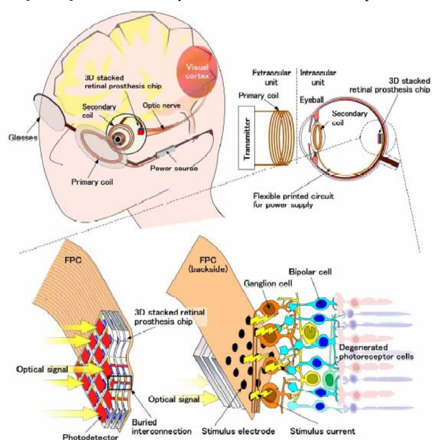


(a) human retina (b) 3D retina chip

Photomicrograph of 3D Artificial Retina Chip



3D Retina Chip Implantation (Retinal Prosthesis) into Human Eye



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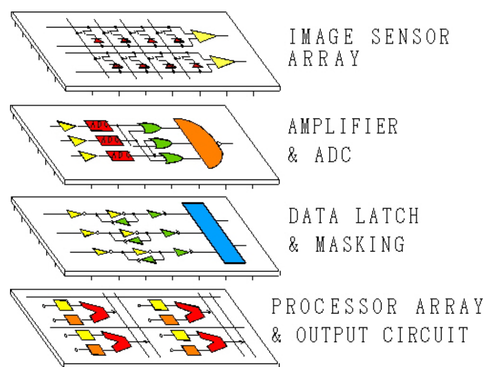
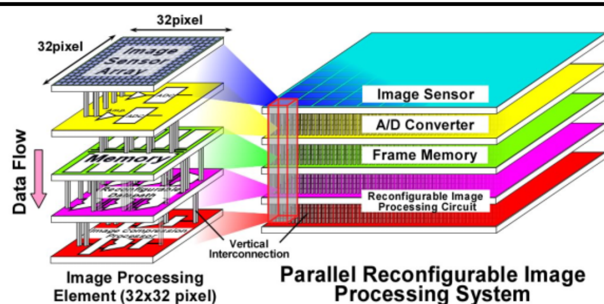
Real-Time Image Processing System with 3D Stacked Structure

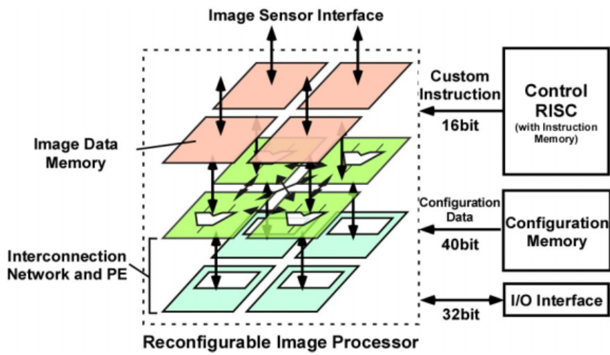


Parallel Reconfigurable Image Processing System with Three Dimensional Structure



- Reconfigurable architecture enables high speed image processing with high flexibility
- Three dimensional structure realizes scalable parallel architecture
- Bandwidth problem is solved

Configuration of Designed Dynamically Reconfigurable Image Processor



Configuration of RISC Processor for Reconfiguration Control

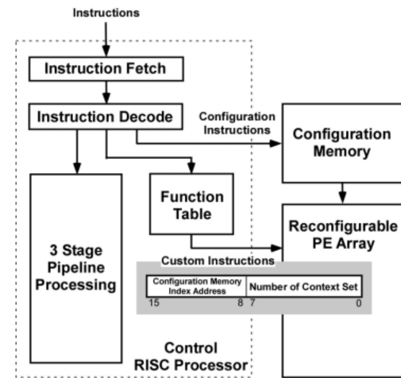
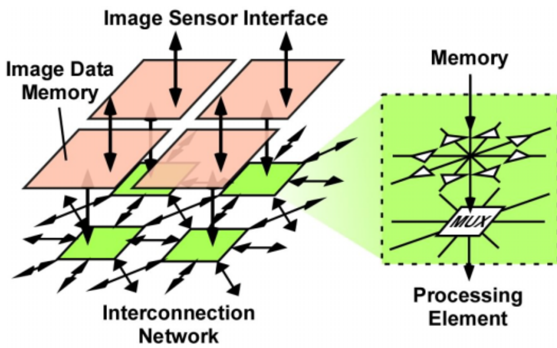
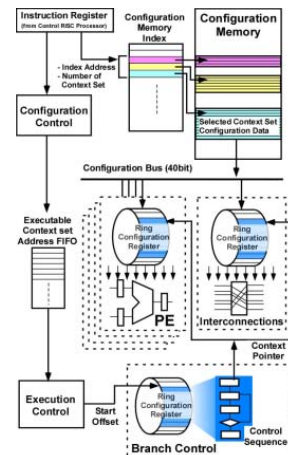


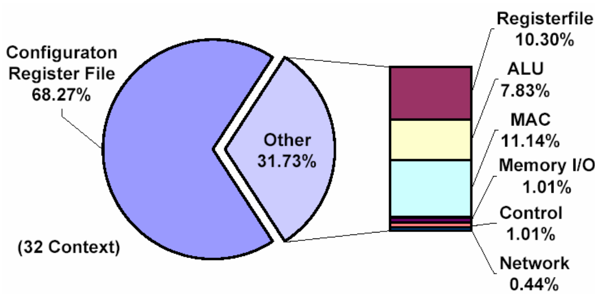
Image Data Memory and Interconnection Network



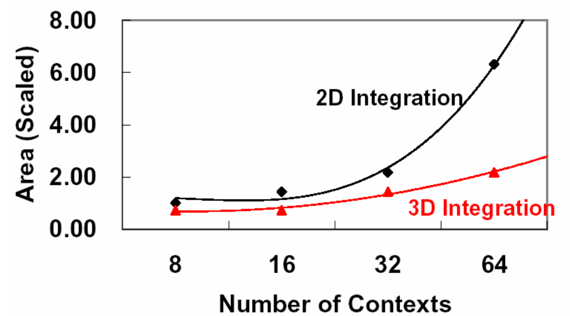
Hierarchical Multi-Context Configuration Architecture



Breakdown of the processing element cell area



Area Evaluation with 2D and 3D Integration for Change of Number of Contexts



Summary

1. 3D integration technologies based on wafer-to-wafer bonding and chip-to-wafer bonding developed in Tohoku University were briefly described.
2. Various 3D LSI test chips with three and ten layers were successfully fabricated and their basic operations were confirmed. New applications for 3D LSI such as robot eye and retinal prosthesis were demonstrated.
3. Reconfigurable image processor with three-dimensional structure was proposed. This image processor can realize wide bandwidth memory access and the scalable architecture simultaneously. It was confirmed from the system simulation that the performance of processor with the determination of the object centroid function is 4.42 times larger than that of the general-purpose microprocessor.