Inductor based Circuit Techniques for Chip-to-Chip Interconnect and Standing Wave Clock Generation

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Outline

• Motivation
• Inductor Based Wireless Chip-Interconnect
• Measurement Results
• Standing-Wave Clock Distribution
• Measurement Results
• Conclusions

on-chip inductor

useful passive element
for *RF circuit.*

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There is few report of
applying to **high-speed digital circuit.**

Inductance cancels capacitive load.
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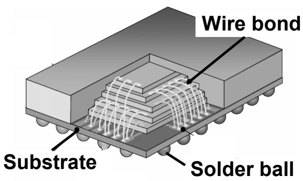
operate faster and reduce power consumption.

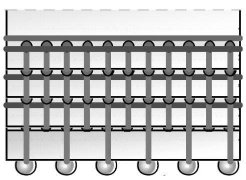
we present two conspicuous cases.

1. Spiral-Inductor Based Wireless Chip-Interconnect

3D Interconnect



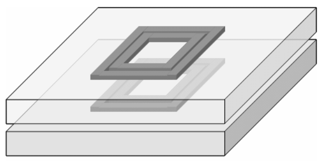
Stacked-Chip with Wire Bond



Micro Bump

Limited bandwidth **Complicated fabrication**

Spiral-Inductor based Interconnect



Instead of "Si Thru Via" and "Micro Bump "

Pros.
• No complicated fabrication
• No ESD protection
• Large bandwidth

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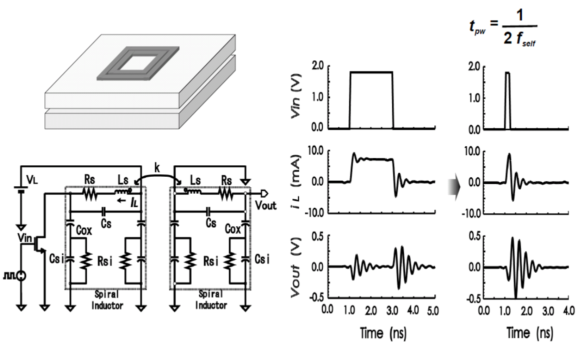
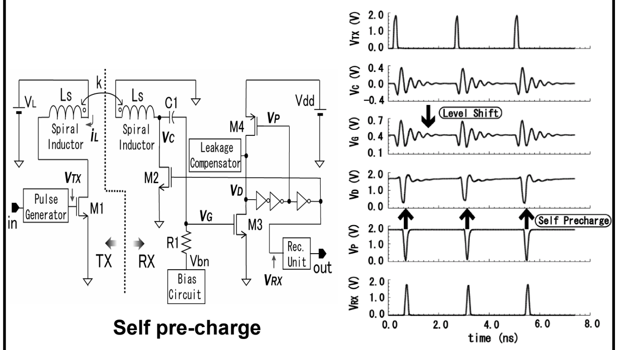
Cons.
• Power consumption
• Clocking Scheme

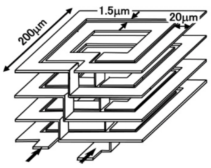
Resonance on Spiral Inductors

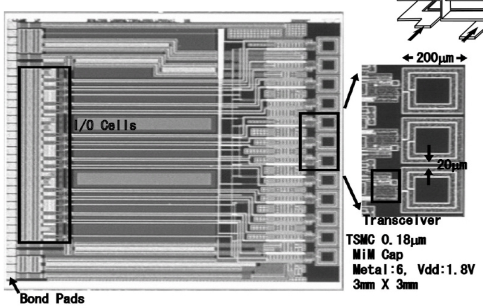


Asynchronous Communication

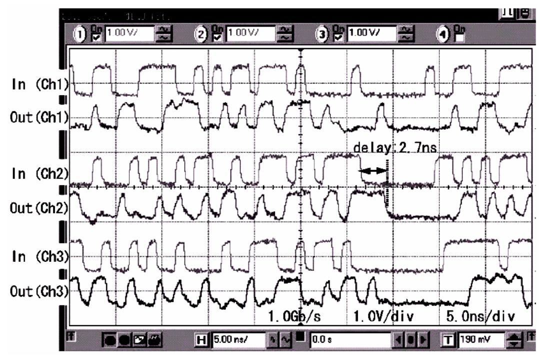


Die Micrograph

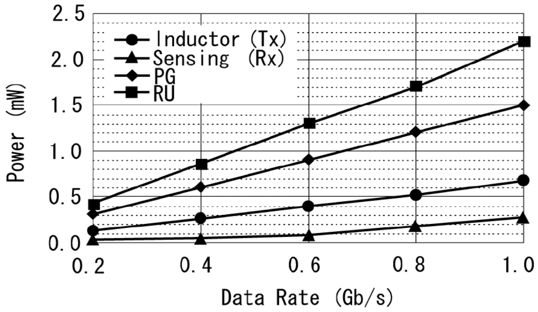




Measured Waveforms



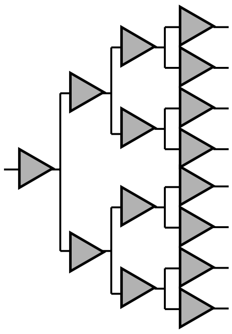
Measured Power Consumptions



2. Standing-Wave Clock Distribution

Clock Distribution Problems

Clock buffer tree



Large latency in deep tree

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Skew/jitter

Large capacitive load, de-skew

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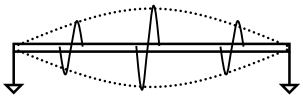
Power dissipation

Standing Wave Clocks



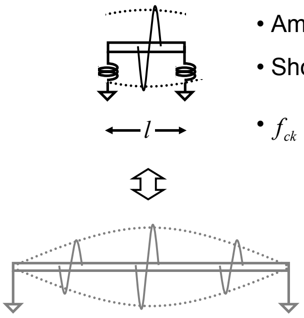
Pros.

- Same phase across TL ⇨ low skew/jitter
- Inductance in TL ⇨ low power

Cons.

- Amplitude varies across TL.
- TL length determines the clock frequency.

Inductively-loaded Standing Wave



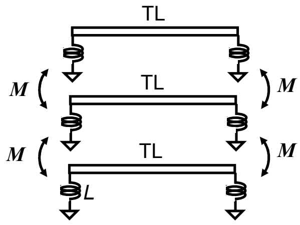
- Amplitude almost constant.
- Shorter length
- $f_{ck} = \frac{1}{2\pi} \frac{Z_0}{L} \tan(\pi - \beta l)$

Z_0 : characteristic impedance

β : phase constant of TL

L : inductance of load

Inductively-Coupled Standing Wave



$f_{ck} = \frac{1}{2\pi} \frac{Z_0}{L_{all}} \tan(\pi - \beta l)$

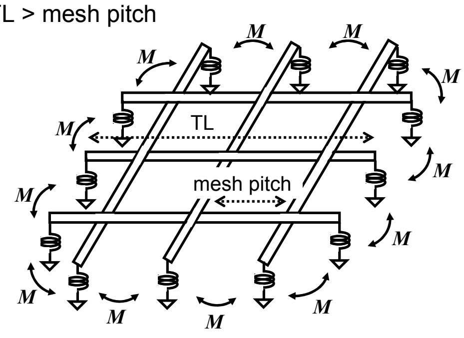
where $L_{all} = (1 + 2k)L$

$k = M / L$

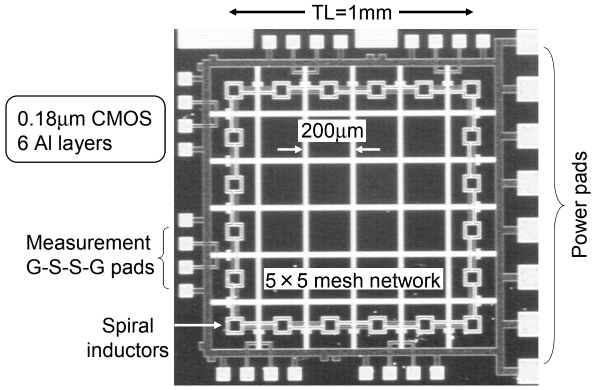
Magnetic coupling synchronizes standing waves.

Low-area-overhead Clock Network

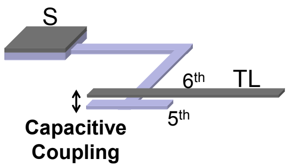
TL > mesh pitch

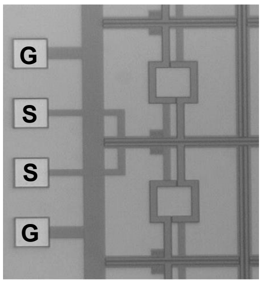


Test Chip



Capacitively-coupled Pad for Measurement



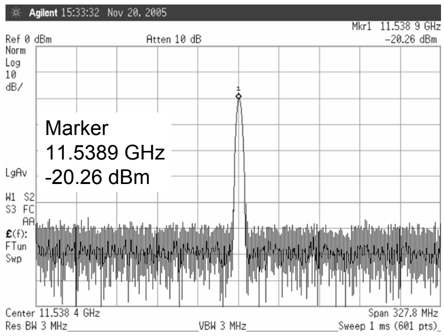


Measured attenuation :

–21dB@ 11.5GHz

(Attenuation minimizes probing influence.)

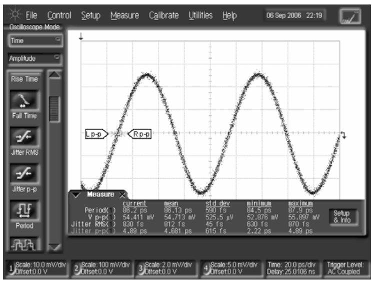
Measured Spectrum



Capacitively-coupled pad attenuation : –21dB@ 11.5GHz

Measured Oscillation Waveform

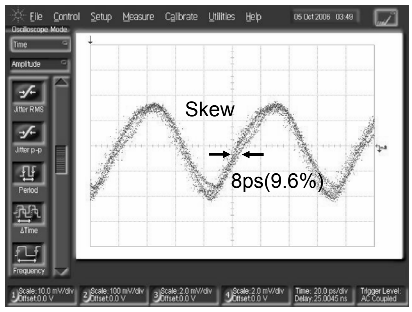
Period : 86.1ps
Jitter(rms) : 0.81ps
Jitter(p-p) : 4.7ps
Amp : 55mVp-p



Capacitively-coupled pad attenuation : –21dB@ 11.5GHz

Amp : 55mVp-p ⇨ 0.6Vp-p

Phase Properties



Four measured clock waves are superimposed.

Conclusions

Wireless Chip-Interconnect

- Power reduction by resonation of inductor coupling.
- Asynchronous Communication with self pre-charging.
- 0.95mW/1.0Gbps/ch was confirmed by the measurements.

Standing-Wave Clock Distribution

- Low-area-overhead and fine-pitch clock network
- Low power of 80mW @ 5 × 5 network, 0.9V
- Low jitter of 4.7ps(p-p) @ 11.5GHz
- Low skew of < 8ps @ 11.5GHz