Low-Noise and Low-Voltage Circuit Techniques for CMOS Analog Design

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1. Introduction

A system on chip (SoC), which has various functions on a LSI, has been developed for a variety of applications by the submicron technologies. Especially, implantable and/or attachable neural sensor chips, which are implemented by the SoC, attract a lot of interest [1]. The neural sensor chip, which includes with a low-noise amplifier, analog-to-digital converter (ADC), transceiver, and so on, needs low-voltage and low-power operation from the point of view as a long-term operation. However, there are many issues for realizing the neural sensor chip utilizing the sub 0.1 μm technologies [2]. One of the issues is a decreasing of the supply voltage. In the low supply voltage, the CMOS analog switch cannot transmit an intermediate voltage level due to increasing the ON resistance of the analog switch. It makes the operation of sample-and-hold difficult in the ADC which is an essential circuit block for realizing the sensor chip. Other issues are the variability of MOSFETs and increasing low-frequency (1/f) noise. The low-noise amplifier for detecting very small neural signals with μV range is one of the most significant circuits in the sensor chip; however, the detection of the small signals becomes difficult by these issues.

This paper presents low-noise and low-voltage circuit techniques for CMOS analog design. These are low-voltage circuit technique utilizing the switched op-amp and grounded switch, and the low-noise circuit techniques of autozero and chopper stabilization operating in the low supply voltage.

2. Low-Noise Amplifier

2.1. Basic Concept

The autozeroing and chopper stabilization techniques are widely used for reducing 1/f noise and the dc-offset voltage [3]. The principle of the autozeroing technique is illustrated in Fig. 1. The autozeroing technique is sampling the noise of the op-amp, such as the dc offset Voff and 1/f noise Vfn, at a null input; and then subtracting the effect of noise from the input signal using a sample-and-hold (S&H) circuit. Thus, the autozeroing technique can reduce the low-frequency noise of the amplifier. One disadvantage of autozeroing is an increase of the baseband noise floor, which is caused by the aliasing of the wideband noise that is inherent to the sampling process.

The principle of the chopper stabilization technique is shown in Fig. 2. Chopper stabilization, based on a modulation technique, converts the frequency range of an input signal to the higher frequency range of a chopping frequency fc where the dominant noise is a white noise, and then demodulates it back to the baseband after amplification. To remove the noise demodulated within higher frequency range than the chopper frequency and to obtain a low spurious signal, the high order low pass filter (LPF) is required. Using both autozeroing and chopper stabilization techniques together contributes to a reduction of both the baseband noise floor and the modulated noise at the chopper frequency [4] because the autozeroing removes the dc-offset, and the chopper stabilization decreases the baseband noise.

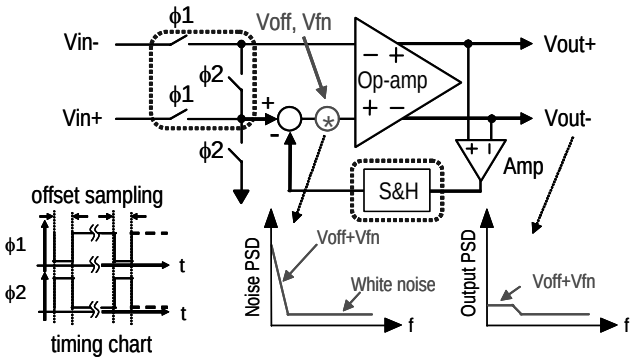

Fig.1 Principle of autozeroing technique.

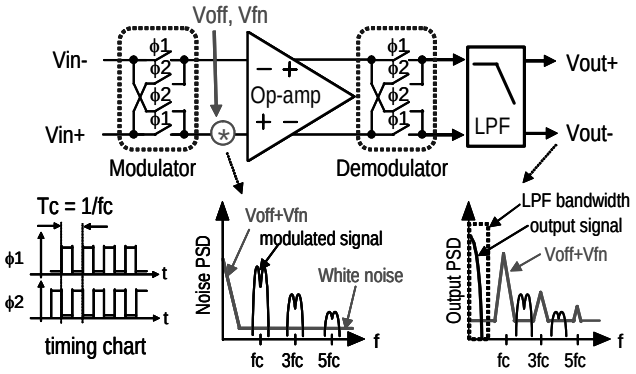

Fig.2 Principle of chopper stabilization technique.

2.2. Architecture

A conceptual diagram of the proposed low-noise amplifier, based on a switched-capacitor amplifier, employing the techniques of autozeroing and chopper stabilization is shown in Fig. 3. In order to overcome the issue of the CMOS analog switch operating at a low supply voltage, the switched-capacitor amplifier was

implemented by a multi-output switched op-amp.

The chopper modulators (CHP1, CHP2) with the virtual grounds are implemented by simple CMOS analog switches as shown in Fig. 3, because a voltage level of virtual ground is possible to set to any level and the input signal amplitude is small. The proposed architecture requires inserting the extra modulator (CHP2) into the feedback loop to modulate the output signal previously demodulated by the CHP3, however the incremental area of the CHP2 is almost negligible. On the other hand, the CHP3 demodulator placed outside the virtual ground cannot be formed with analog switches because of large output amplitude. The CHP3 is therefore implemented by a switched op-amp. The CHP1, CHP2 and CHP3 are switched by the complementary clock signals of $\phi 1$ and $\phi 2$.

The multi-output switched op-amp is also able to configure the autozeroing scheme. During the $\phi 0$ phase, the output of the switched op-amp are connected to their input using dotted lines as shown in Fig. 3, forming a voltage follower. The paths are activated on the initial $\phi 0$ phase and the detected dc offset voltage is stored into a hold capacitor C2; accordingly, the autozeroing operation cancels the dc offset. If the offset sampling is periodically carried out, low-frequency noise can also be reduced.

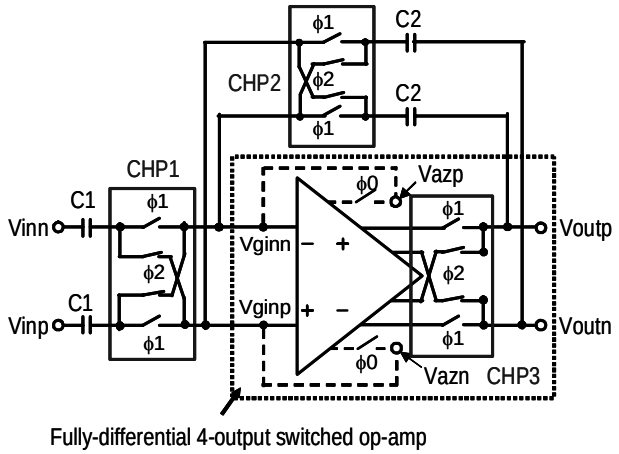

Fig. 3 Conceptual block diagram of the low-noise amplifier based on the techniques of autozeroing and chopper stabilization.

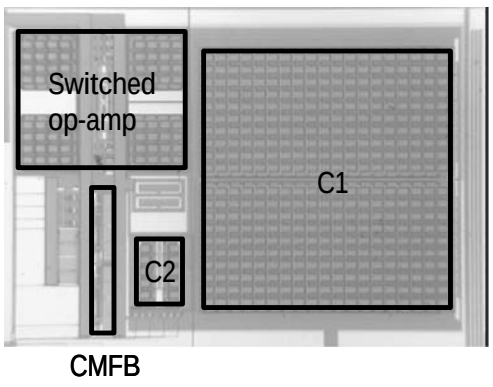

Fig. 4 Micrograph of the low-noise amplifier.

2.3. Experimental Results

A test chip of the low-noise amplifier base on chopper stabilization and autozeroing technique is fabricated in a 0.18 μm CMOS process, with nominal NMOS and PMOS threshold voltages of about 0.42 V and -0.5 V, respectively. The micrograph of the test chip is shown in Fig. 4. The chip area is 1100×800 μm^2. The feedback capacitor C1 and C2 are implemented in 80-pF and 2-pF, respectively.

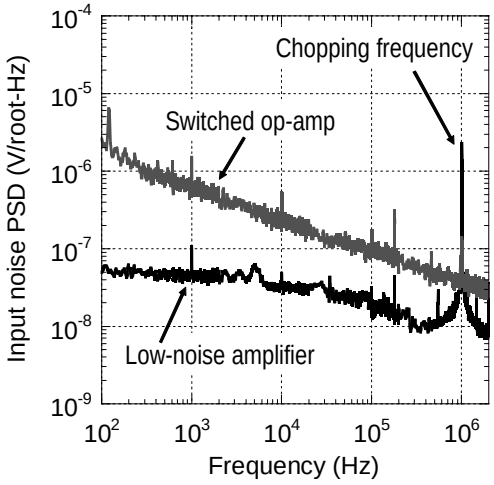

Fig. 5 Measured input noise PSD versus frequency of the switched op-amp and the low-noise amplifier with autozeroing and chopping operation.

The input noise PSD of switched op-amp and low-noise amplifier is shown in Fig. 5. The low-noise amplifier operated with 1-MHz chopping frequency and 5-μs autozeroing time at a supply voltage of 1 V. The input noise of switched op-amp shows a typical 1/f noise spectrum, and the noise PSD is 2.5-μV/√Hz at 100 Hz. The proposed low-noise amplifier suppressed the noise PSD to less than 50 nV/√Hz. The low-noise amplifier achieved 32-dB voltage gain and 2-MHz cut-off frequency at 1-MHz chopping operation.

Table I Comparison of the reference op-amps and this work.

	This work	Ref. [4]	Ref. [5]
Supply voltage (V)	1.0	5.0	1.0
Autozeroingfrequency (kHz)	<0.001	7.5	-
Chopping frequency (kHz)	1000	15	-
Input noise PSD (nV/vHz)	50	20	360
Input offset voltage (μV)	290	3	3000
Power consumption (mW)	0.5	4.0	0.2
Chip area (mm^2)	0.88	0.67	0.81
FOM × 10^3	45	18.7	17.1

The performance comparison of referred amplifiers and proposed amplifier is summarized in Table I. The operating time of initialized amplifier was more than 1 hour, thus the autozeroing frequency is described as less

than 1 Hz. The referred amplifiers focused on a noise reduction or a low voltage operation. We defined the figure of merit (FOM) focused on noise, power and area; the equation is as follows:

$$FOM = 1 / N \times S \times P, \quad (1)$$

where N is the noise density, P is the power dissipation and S is the chip area. The FOM of proposed amplifier achieved 2.4-times larger than the referred amplifiers [4, 5].

3. Successive Approximation ADC

3.1. Concept for low-voltage operation of the ADC

To solve the low supply voltage issue, which is an increasing ON resistance of the floating CMOS analog switch, a switched op-amp technique has been developed for the pipeline ADC [6]. The switched op-amp, which is equipped with grounded switches in the output stage, can change the output impedance of the output stage from low to high at a low supply voltage. Thus the sample-and-hold operation in the ADC has been realized with the switched op-amp.

As the other technique, a capacitor-array digital-to-analog converter (DAC) using grounded switches has also been proposed [7]. The DAC provides a reference voltage to a comparator, which compares the input voltage and the reference voltage, and the operation is independent of the input voltage range and the supply voltage. Therefore the ADC utilizing the DAC can use the method of a successive approximation at a low supply voltage.

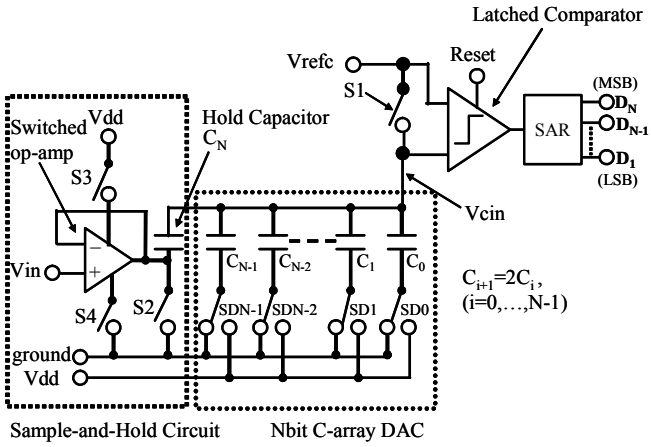

Fig. 6 Block diagram of the Nbit ADC with the switched op-amp and grounded switches.

3.2. Architecture

The proposed architecture of a successive approximation ADC based on the capacitor-array is shown in Fig. 6. The ADC includes a capacitor-array DAC, a successive approximation register (SAR), a latched comparator and a sample-and-hold (SH) circuit. The N bit DAC implemented by a binary-weighted capacitor-array consists of Ci's: $C_{i+1} = 2C_i$ (i = 0 ~ N-1), and C_N as a hold capacitor. The grounded switches SDi (i = 0 ~ N-1), which controlled by the SAR, connect these capacitors and the power supply line of Vdd or that of ground. The SH circuit is composed of the switched op-amp configured as voltage follower and the hold capacitor C_N, as shown in Fig. 6.

In this architecture, since the offset voltage of the comparator is constant, it does not cause non-linearity error of the ADC. Although the parasitic capacitor of the DAC output node gives the attenuation of Vcin, it does not decrease the input voltage range of ADC, and does not cause any offset error and nonlinearity error. Other advantage of the ADC is that the input impedance keeps a high because of the SH circuit implemented by the switched op-amp.

3.3. Circuit Design and Experimental Results

The schematic of the SH circuit with switched op-amp is illustrated in Fig. 7. The input stage of switched op-amp consists of a complementary differential circuit with a rail-to-rail input voltage range, and it can drive an output stage with voltage range from ground to Vdd. The output stage of switched op-amp includes a class-AB buffer and two grounded-switches of Mc3 and Mc4. In the sample mode, the switched op-amp provides an input voltage to the hold capacitor. The output impedance of the buffer changes to high by turning off the grounded-switches S3 and S4 in the hold mode, therefore the input voltage is held on the C_N. This switched op-amp employs the hold capacitor for phase compensation capacitor instead of Miller topology.

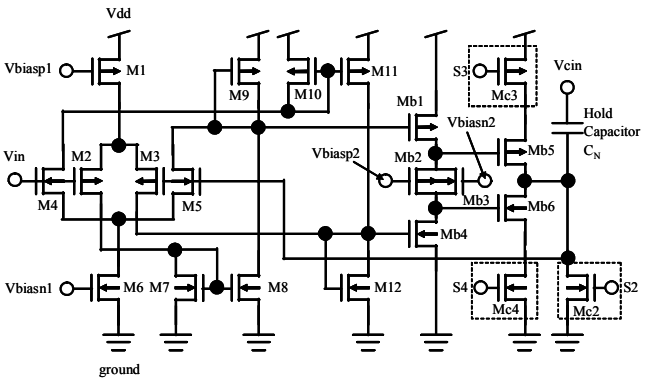

Fig. 7 SH circuit with switched op-amp.

The prototype ADC was fabricated by 0.18 μm mixed-signal CMOS process (Vthn = 0.42 V, Vthp = -0.50 V) with metal-insulator-metal (MIM) capacitor. The photograph of prototype ADC chip is shown in Fig. 8, where the active area is about 1.0 mm^2. Designed parameters are as follows: ADC resolution N = 10-bit, Vdd = 1 V, Vrefc = 0.3 V, the unit capacitor C_0 = 50-fF, MOS size of switch S1 W/L = 100μm/0.18μm and the other switch size W/L = 20μm/0.18μm.

To achieve 10-bit accuracy at a 400-ksps conversion rate, the switched op-amp is designed to have a 60 dB open-loop gain, -3 dB bandwidth of 8 kHz and 6 MHz

unity-gain frequency with a hold capacitance of 51.2 pF (as shown in Fig. 6). In order to reduce power dissipation of the switched op-amp (which is presented in Fig. 7), MOSFET sizes (W/L) of the output buffer Mb5 and Mb6 are set to relatively small values of 15-μm/0.18-μm and 5-μm/0.18-μm respectively. The simulated linearity error of switched op-amp, which operated as the SH circuit, is within ±0.25 mV for a 0.1~0.9 V input voltage range. The slew rate and settling time are 10.0 V/μs and 250 ns respectively, when the input voltage changes from ground to Vdd.

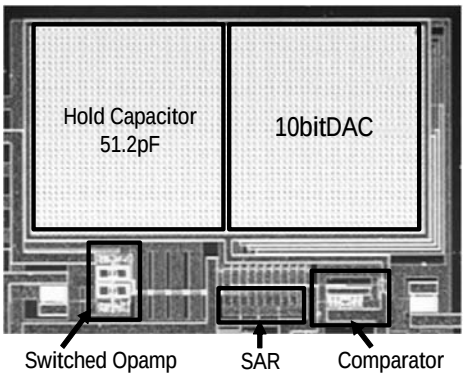

Fig. 8 Chip photograph of the prototype ADC.

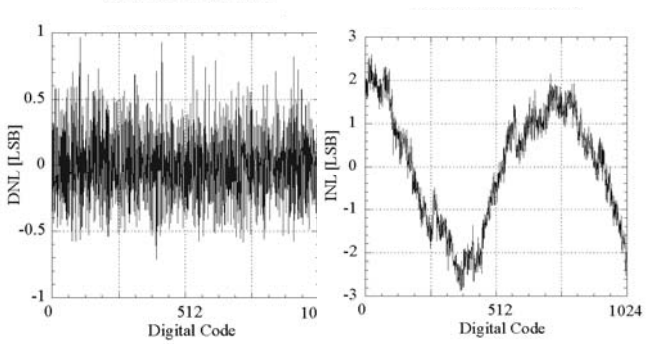

Fig. 9 Measured DNL and INL.

The measured differential and integral nonlinearities (DNL and INL) operated at a 400 kSps are shown in Fig. 9. The largest DNL and INL were less than 0.9 LSB and 2.9 LSB, respectively. The proposed ADC achieved an input voltage range of 800 mV, a sampling rate of 400 kSps, and a power consumption of 0.2 mW at 1 V supply voltage.

The performance comparison between the proposed 10-bit ADC and published successive approximation ADCs is summarized in Table II. In the published ADCs, the low-voltage operation [8] and the improvement of power consumption and accuracy [9] are considered. We introduced a figure of merit (FOM) for ADC considering resolution, speed, power and area; the equation is as follows:

$$FOM = (2^n \times BW / P) \times (2^n / S), \quad (2)$$

where n is the resolution in bit, BW is the sampling rate, P is the power consumption and S is the chip area. The FOM of proposed ADC is about 7-times larger than the referred ADC.

Table II Comparison of the ADC performances.

	This work	Ref. [8]	Ref. [9]
Resolution (bit)	10	8	12
Supply voltage (V)	1.0	1	5.0
Power consumption (mW)	0.2	0.34	15
Chip area (mm^2)	1.0	3.24	1.5
Sampling Rate (kSps)	400	50	1000
FOM	2048	37.6	273

4. Conclusion

In this paper, a low-noise circuit technique based on autozeroing and chopper stabilization techniques and low-voltage circuit technique are presented. The key of noise reduction at a low supply voltage are the multi-output switched op-amp, and the chopper modulator operating at the virtual ground level. The amplifier utilizing the low noise techniques has achieved 50-nV/√Hz noise PSD, 52 dB THD, 88-dB dynamic range at 1 V supply voltage. The key techniques of low-voltage operation are also the switched op-amp and the grounded switch. The prototype 10-bit successive approximation ADC utilizing grounded switches and switched op-amp has achieved sampling rate of 400 kSps and power consumption of 0.2 mW at 1 V supply voltage.

References

[1] K. D. Wise et al., "Wireless Implantable Microsystems: High-Density Electronic Interfaces to the Nervous Systems", Proceedings of The IEEE, vol. 92, No.1, pp.76-97, Jan. 2004.

[2] "International Technology Roadmap for Semiconductors 2005 Edition", ITRS, Executive Summary, 2005.

[3] C. C. ENZ et al., "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proceedings of The IEEE, vol. 84, No. 11, pp.1584-1614, Nov. 1996.

[4] A. T. K. Tang, "A 3uV-Offset Operational Amplifier with 20nV/√Hz Input Noise PSD at DC Employing both Chopping and Autozeroing", IEEE ISSCC Digest of Technical Papers, pp.386-387, Feb.2002.

[5] J. F. Duque-Carrillo et al., "1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology", IEEE Journal of Solid State Circuits, vol.35, No. 1, pp.33-44, Jan 2000.

[6] M. Waltari et al., "1-V 9-bit pipelined switched-opamp ADC", IEEE J. Solid-State Circuits, vol. 36, No.1, pp.247-250, pp.129-134, Jan. 2001.

[7] J. Sauerbrey et al., "A 0.5V, 1mW Successive Approximation ADC", Proc. 28th Euro. Solid-State Circuits Conf., September 2002, Firenze, pp.247-250.

[8] S. Mortezapour et al., "A 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process", IEEE J. Solid-State Circuits, vol.35, No.4, pp.642-646, April 2000.

[9] G. Promitzer, "12-b Low-Power Fully Differential Switched Capacitor Noncalibrating Successive Approximation ADC with 1MS/s", IEEE J. Solid-State Circuits, vol.36, No.7, pp.1138-1143, July 2001.