Low-Noise and Low-Voltage Circuit Techniques for CMOS Analog Design

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Outline

1. Introduction
2. Basic concept
   - Low-voltage technique
   - Low-noise technique
3. Low-noise amplifier
4. Low-voltage SA ADC
5. Summary

Introduction

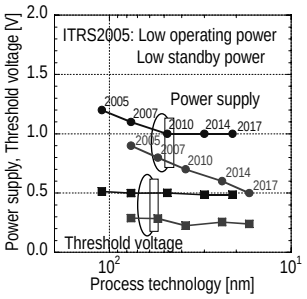
CMOS technology innovation

Advantage

- High-speed operation
- Lower power consumption
- Shrinking chip area

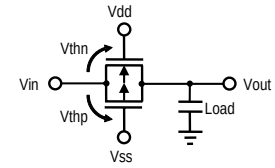
Disadvantage

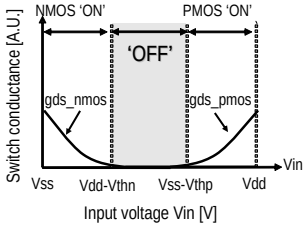
- Power supply voltage reduction
  - -Analog switch issue
  - -S/N deterioration
- Vth variation
- 1/f noise



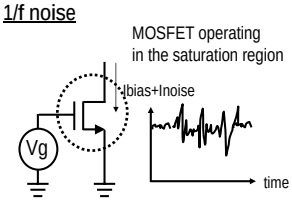
Issues of CMOS analog design

CMOS analog switch

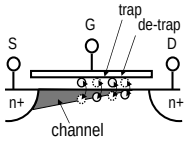




1/f noise



Large 1/f-noise



Objectives

Proposals for low-voltage and low-noise circuit techniques to realize a CMOS analog design in a state of the art process technology.

- Noise reduction ➡ •Autozeroing •Chopper stabilization
- Low voltage ➡ •Switched op-amp •Grounded switch •Rail-to-rail signal swing

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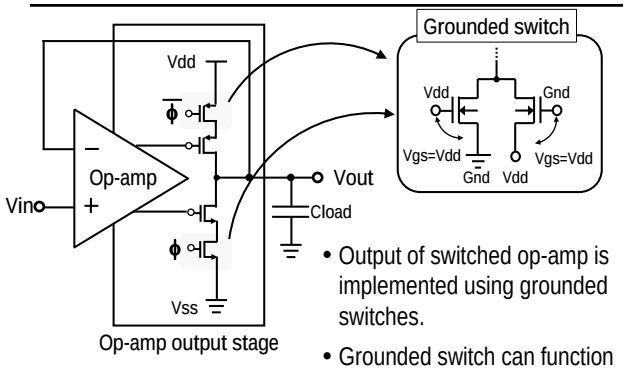
Grounded switch



- Output of switched op-amp is implemented using grounded switches.
- Grounded switch can function properly when Vdd<|Vthp|+Vthn

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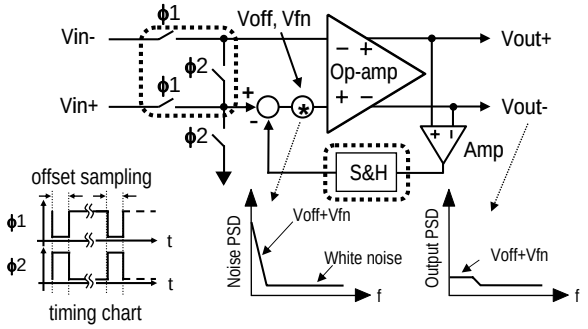
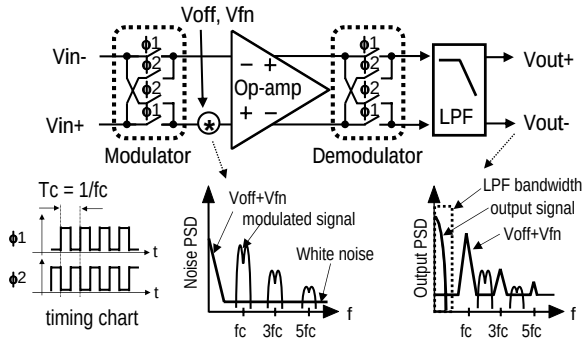
Autozeroing



- Increment of baseband noise floor
- Bootstrap technique or low-Vth device is required

Chopper stabilization



- Large noise power remains at a chopping frequency
- Bootstrap technique or low-Vth device is required

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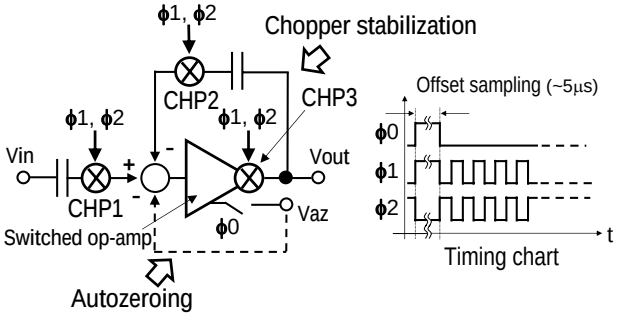
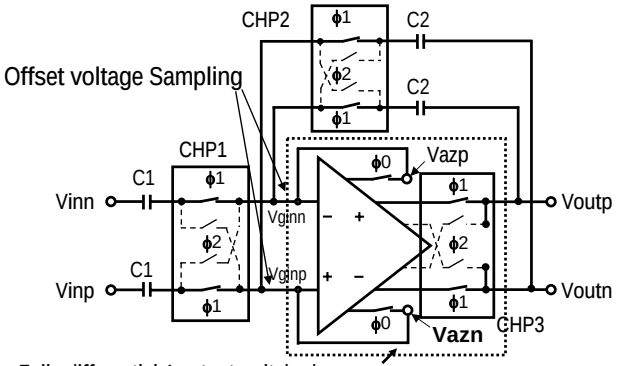
Low-noise low-voltage amp: Concept



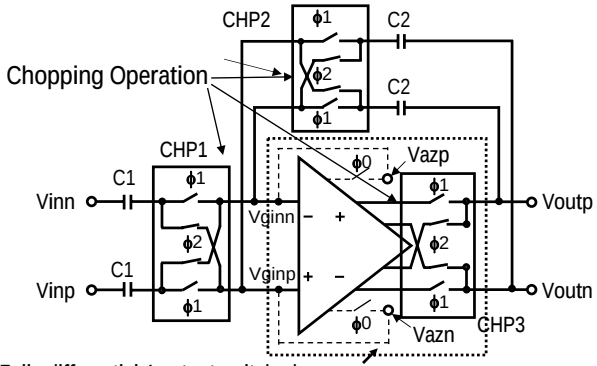
- Switches (CHP1,2) in the virtual ground
- Chopper (CHP3) implemented by switched op-amp
- Use both noise reduction techniques

Proposed autozeroing technique



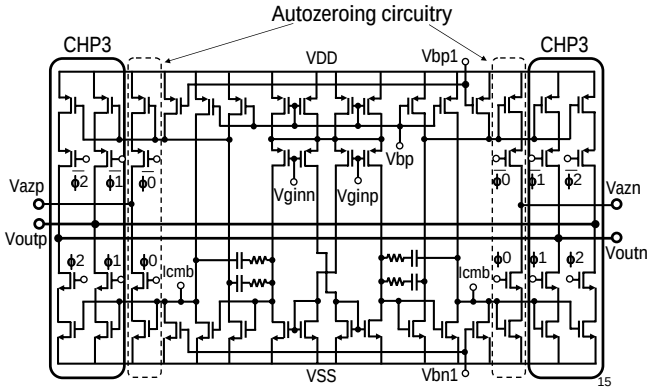
Fully-differential 4-output switched op-amp

Proposed chopper stabilization

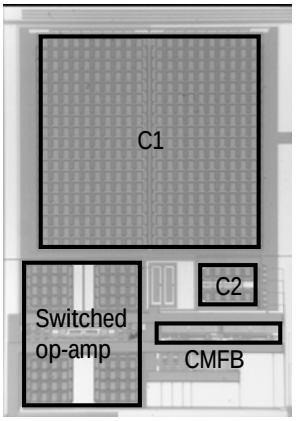


Fully-differential 4-output switched op-amp

Switched op-amp



Chip micrograph



Process

0.18μm CMOS,
1-Poly/6-Metal/MiM-Cap
0.42V:NMOS Vth
0.5V:PMOS Vth

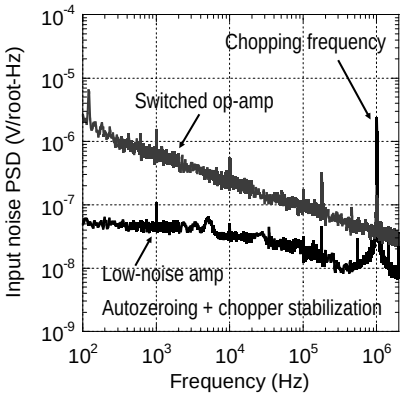
Supply Voltage

1V

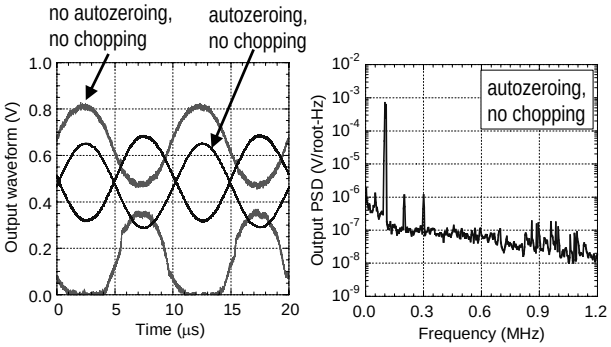
Area

800 x 1100 μm^2

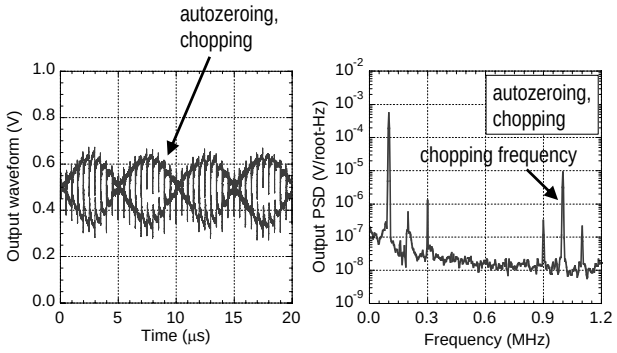
Input noise PSD



Amplifier output 1/2



Amplifier output 2/2



Comparison of amplifier performances

	This work	ISSCC2002[1]	JSSC2000[2]
Supply voltage (V)	1.0	5.0	1.0
Autozeroing frequency (kHz)	< 0.001	7.5	-
Chopping frequency (kHz)	1000	15	-
Input noise PSD (nV/√Hz)	50	20	360
Power consumption (mW)	0.5	4.0	0.2
Chip area (mm^2)	0.88	0.67	0.81
FOMx10^3	45	18.7	17.1

$$\text{Figure of Merit} = \frac{1}{\text{Noise PSD} \times \text{Power} \times \text{Area}}$$

[1]A. T. K. Tang, "A 3uV-Offset Operational Amplifier with 20nV/√Hz Input Noise PSD at DC Employing both Chopping and Autozeroing", IEEE ISSCC Digest of Technical Papers, pp.386-387, Feb.2002.
[2]J. F. Duque-Carrillo et al., "1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology", IEEE Journal of Solid State Circuits, vol.35, No. 1, pp.33-44, Jan 2000.

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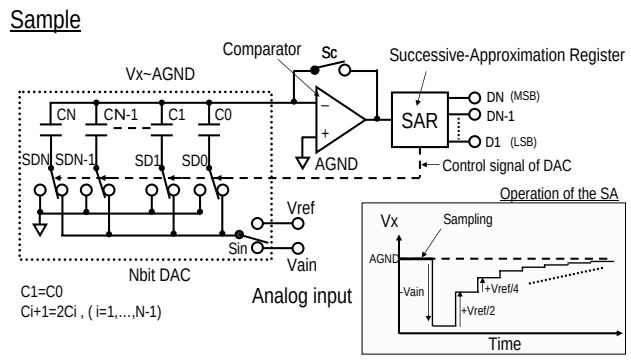
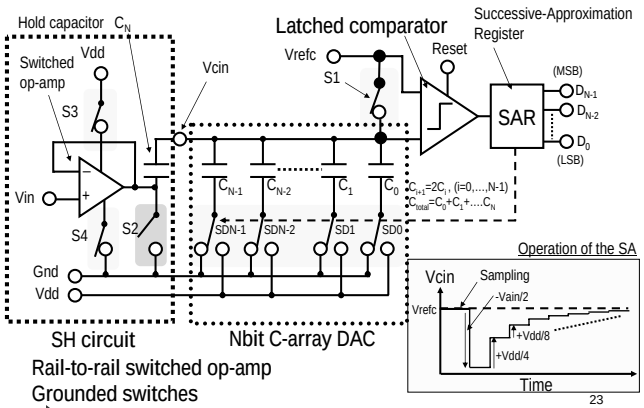
SA ADC based on charge-redistribution



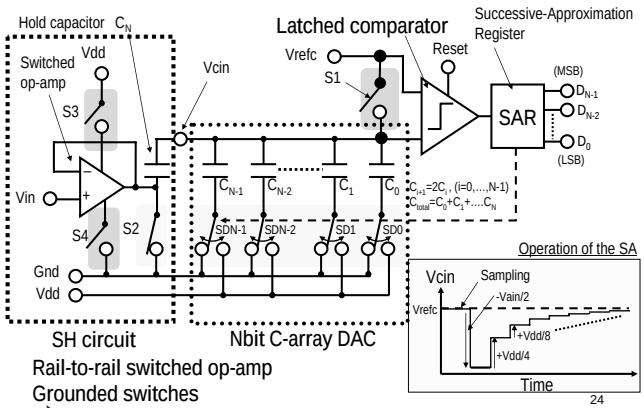
CMOS analog switches can't function properly when Vdd<|Vthp|+Vthn

Proposed SA ADC with rail-to-rail input



Rail-to-rail switched op-amp
Grounded switches
➡ Rail-to-rail input range, low-voltage operation

Proposed SA ADC with rail-to-rail input



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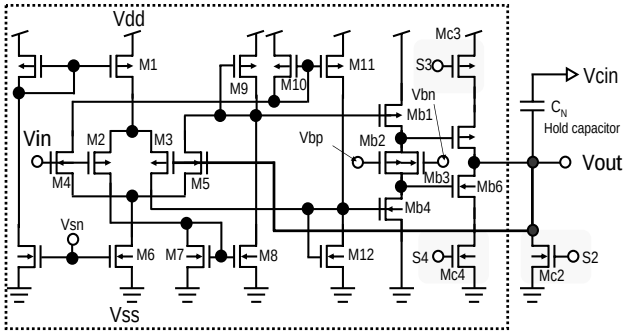
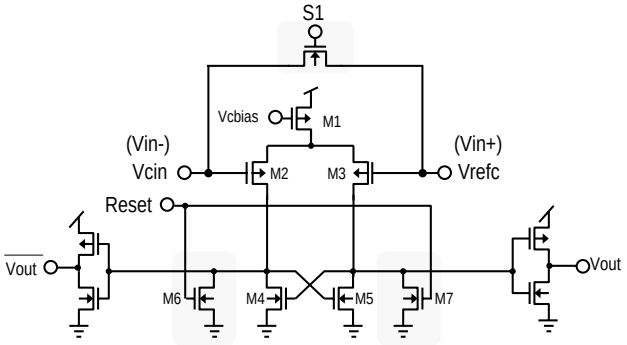
Grounded switches
➡ Rail-to-rail input range, low-voltage operation

Sample and hold circuit

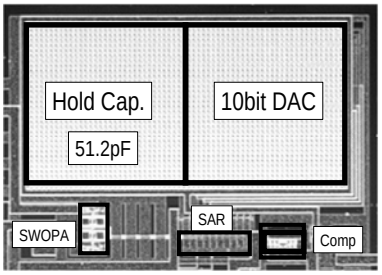


Switched op-amp

Latched comparator



Chip micrograph



Technology

0.18um CMOS Process
1P 6M MIM-Cap
Vthn: 0.42V
|Vthp|: 0.50V

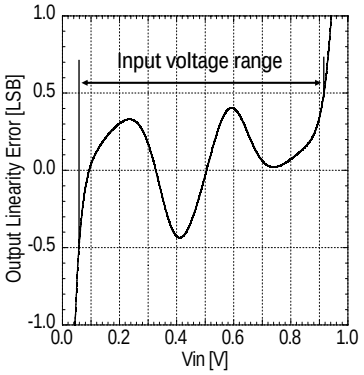
Chip area

1.25 x 0.85 mm^2

Supply voltage

1 V

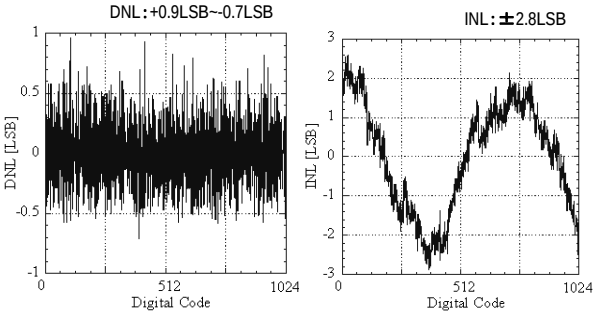
Linearity error of SH circuit



Specifications

Linearity error: +/-0.25mV
Input range: 0.05V~0.9V
Power:170uW
Supply voltage:1V

Differential and Integral nonlinearities



Sampling rate:400kSps
Input voltage range: 50mV~870mV

Comparison of ADC performance

	This work	JSSC 2000[1]	JSSC 2001[2]
Supply voltage (V)	1.0	1.0	5.0
Resolution (bit)	10	8	12
Sampling rate (kSps)	400	50	1000
Power consumption (mW)	0.20	0.34	15
Chip area (mm^2)	1.0	3.24	1.5
FOM	2048	37.6	273

Figure-of-Merit defined by: $\frac{2^n \cdot \text{Sampling Rate}}{\text{Power}}$

[1] S. Mortezapour et al, "A 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process", JSSC, vol.35, pp.642-250646, April 2000.
[2] G. Promitzer, "12-b Low-Power Fully Differential Switched Capacitor Noncalibrating Successive Approximation ADC with 1MS/s", JSSC, vol.36, pp.1138-1143, July 2001.

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Summary

Low-noise and low-voltage circuit techniques are presented

Key technique:

Autozeroing and chopper stabilization
Multi-output switched op-amp
Grounded switch
Rail-to-rail input range

- Low-noise amp achieved 50nV/√Hz noise PSD, 52dB THD and 88dB DR at 1V supply voltage
- 10bit SA ADC achieved 400kS/s sampling rate, 200uW power dissipation at 1V supply voltage