Development of Reliable High-*k* Gate Dielectrics for Scaled MOSFETs

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1. Introduction

In this COE project, the subject of our group is the research and development of future reliable gate dielectrics. The subject includes atomic-layer-deposition (ALD) of silicon nitride, ALD high–*k* gate dielectrics, and plasma nitrided SiON gate dielectrics, etc. Here, static and dynamic bias temperature instability in p- and n-MOSFETs having plasma nitrided SiON gate dielectrics was investigated in detail. ALD Si nitride/SiO_2 gate dielectrics were applied to future scaled DRAM. ALD growth of HfO_2 was also investigated by the alternate exposure of tetrakis diethylmethylamino hafnium and water on both Si and Ge substrates.

2. Static bias temperature instability (BTI)characteristics

Bias temperature instability (BTI) in MOSFETs has emerged as one of the most critical reliability issues with scaling down of gate-dielectric thickness. Based on the reaction-diffusion (R-D) model, the degradation of device performance is widely accepted to be caused by interface trap generation (ΔN_{it}) and oxide charge buildup (ΔN_{ot}). To reveal the detail mechanism of BTI, N_{it} and N_{ot} should be measured accurately and separately. For this purpose, we proposed a modified direct-current current-voltage (DCIV) method [1]. By subtracting the DCIV current measured at $V_s=V_d=0$ from that measured at $V_s=V_d=V_e(\neq 0)$ with carefully selecting a suitable V_e value, the direct-tunneling-current effect of the ultrathin gate dielectrics can be minimized, leading to a clear DCIV peak. Figure 1 shows the configuration for DCIV measurement and the typical modified DCIV curves. Here, N_{it} can be calculated from the DCIV peak height while ΔN_{ot} is closely related to the peak position shift. Moreover, DCIV curves recorded at different temperatures were found to give a similar N_{it} value, leading to the simplification of the procedure for temperature dependence studies.

The above modified DCIV method (Figs. 2 and 3) and a conventional subthreshold characteristic measurement (Fig. 4) were applied to study negative BTI of pMOSFETs with ultrathin plasma-nitrided SiON gate dielectrics [2]. The nitrogen peak is around the middle of the base SiO_2 (2 nm) and the concentrations are 9%, 12% and 15% for samples 1, 2, and 3, respectively. We found that during the NBT stress, ΔN_{ot} is not linearly related to ΔN_{it} (Figs. 2 and 3). At the earlier stress times, ΔN_{it} dominates the threshold voltage shift (ΔV_{th}) and ΔN_{ot} is negligible. At the longer stress times, ΔN_{it} deviates from the power-law time dependence, showing a saturation effect (Fig. 2). On the other hand, ΔN_{ot} still has a power-law dependence on stress time so that the contribution of ΔN_{ot} to ΔV_{th} increases (Fig. 3). Increasing the nitrogen concentration of the plasma-nitrided SiON gate dielectric from 9 to 15% did not detectably enhance the NBTI while the suppression of boron penetration and the EOT reduction have been significantly improved. It indicates that plasma-nitrided SiON is a superior gate dielectric from the viewpoint of NBTI.

3. BTI characteristics under high-frequency bipolar gate bias

NBTI of p-MOSFETs with ultrathin SiON gate dielectric has been investigated under various gate bias configurations [3-6]. The NBT-induced ΔN_{it} under unipolar bias is essentially lower than that under static bias, and is almost independent of the stress frequency up to 10 MHz (Fig. 5). On the contrary, ΔN_{it} under bipolar pulsed bias of frequency larger than about 10 kHz is significantly enhanced and exhibits a strong frequency dependence (Fig. 6). The enhancement was found to be mainly governed by the fall time (t_F) of the pulse waveform (Fig. 7), namely, the transition time of the silicon surface potential from strong accumulation to strong inversion, rather than the pulse rise time (t_R) and the pulse duty factor (D). The enhancement decreases significantly with t_F increasing, and is almost eliminated when t_F is larger than ~ 60 ns. The degradation enhancement is attributed to the transient electrons trapped in the interface states upon switching of the silicon surface potential from accumulation to inversion.

4. Application of ALD Si niutride/SiO_2 gate dielectrics to future DRAMs

ALD of Si nitride is one of the key technologies for the next generation gate dielectrics [7,8]. ALD Si-nitride/SiO_2 stack gate dielectrics were applied to high-performance transistors for future scaled DRAMs [9]. The stack gate dielectrics of the peripheral PMOS transistors excellently suppress boron penetration (Fig. 8). ALD stack gate dielectrics exhibit only slightly worse negative-bias temperature instability (NBTI) characteristics than pure gate oxide (Fig. 9). Enhanced reliability in NBTI was achieved compared with that of plasma-nitrided gate SiO_2 (Fig. 9). Memory-cell (MC) NMOS transistors with ALD stack gate dielectrics show slightly smaller junction leakage than those with plasma-nitrided gate SiO_2 in a high-drain-voltage region, and have identical junction leakage characteristics to transistors with pure gate oxide (Fig. 10). MCs having transistors with ALD stack gate dielectrics and those with pure gate oxide have the identical retention-time distribution (Fig. 10). Taking the identical hole mobility for the transistors with ALD stack gate dielectrics to that for the transistors with pure gate oxide both before and after hot carrier injection [8] into account, the ALD stack dielectrics are a promising candidate for the gate dielectrics of future high-speed, reliable DRAMs.

5. Atomic-Layer-Deposition of HfO_2 on Si and Ge Substrates

We have developed ALD growth of ZrO_2 on Si substrate using zirconium tertiary-butoxide and water [10,11]. This time, ALD growth of HfO_2 was investigated on both Si and Ge substrates by the alternate exposure of tetrakis diethylmethylamino hafnium (termed as TDEAH) and water [12]. Capacitance–voltage (C-V) characteristics on the bare Si and on the chemically oxidized Si show no hysteresis and *k*-value of 12-14 (Fig. 11). MOSFETs with the ALD HfO_2 gate dielectrics on Si substrate were demonstrated using a simple one-mask fabrication process (Fig. 12). Stoichiometric HfO_2 can be deposited on Ge, whereas further studies are necessary to improve the quality.

6. Conclusion

For the development of future reliable gate dielectrics, reliability of plasma nitrided SiON gate dielectics was studied in detail by the measurements of static and dynamic bias temperature instability. Applicability of ALD Si-nitride/SiO_2 stack gate dielectrics to future scaled DRAMs was also investigated. Moreover, ALD growth of HfO_2 was investigated on both Si and Ge substrates with TDEAH and water.

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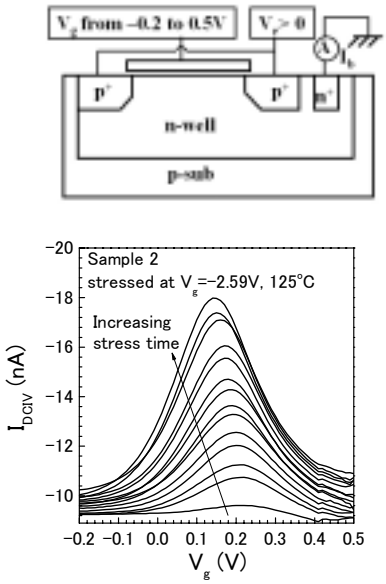

Figure 1 (top) Bias configuration of DCIV measurement. (bottom) Typical modified DCIV curves of a pMOSFET with ultrathin SiON gate dielectric before and after stress.

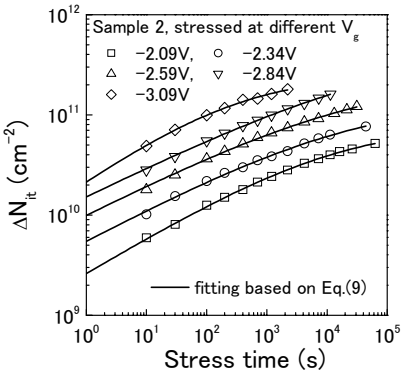

Figure 2 Stress time evolution of interface trap generation (ΔN_{it}) for sample 2 stressed at 125°C at different voltages. Fitting lines are also shown.

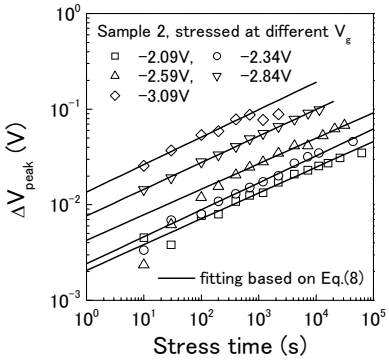

Figure 3 Stress time evolution of DCIV peak position shift (ΔV_{peak}) for sample 2 stressed at 125°C at different voltages and linear fitting.

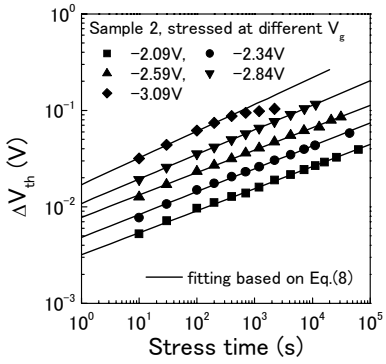

Figure 4 Stress time evolution of threshold voltage shift (ΔV_{th}) for sample 2 stressed at 125°C at different voltages, and linear fitting based on assumption of the power-law dependence.

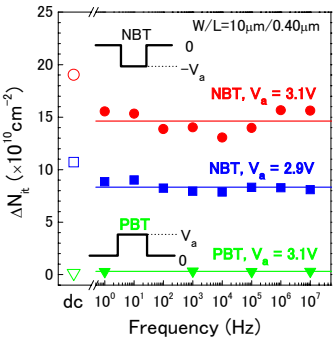

Figure 5 Interface trap generation ΔN_{it} as a function of stress frequency at different stress voltage V_{stress}, under unipolar pulsed stress (L=0.40μm) for a pMOSFET with plasma-nitrided SiO_2 gate dielectrics. Stressed at 125°C for 10^3s. The data of dc stresses are also shown for comparison, whose nominal stress time is 500s. Inset is a schematic waveform applied on the gate.

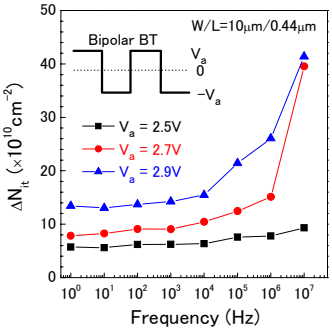

Figure 6 Interface trap generation ΔN_{it} as a function of stress frequency at different stress voltage V_{stress}, under bipolar pulsed stress (L=0.44μm) for a pMOSFET with plasma-nitrided SiO_2 gate dielectrics. Stressed at 125°C for 10^3s.

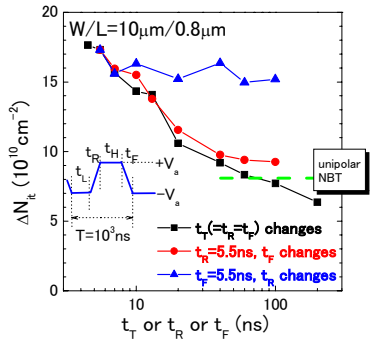

Figure 7 Interface trap generation ΔN_{it} as a function of t_R (or t_F) under bipolar stresses at 10^6 Hz with a trapezoidal waveform. Inset shows a schematic waveform to define t_L, t_R, t_H and t_F for a pMOSFET with plasma-nitrided SiO_2. Devices have size of W/L= 10μm/0.8μm and are stressed at 125°C for 10^3s. For comparison, ΔN_{it} under unipolar stress with a square waveform ($t_T = t_R = t_F = 4.5$ ns) is also shown.

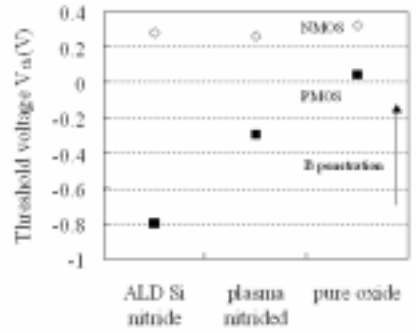

Figure 8 V_{th} of peripheral NMOS and PMOS transistors. L/W=1μm/10μm.

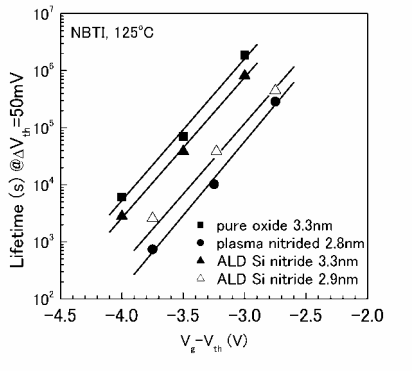

Figure 9 Device lifetime as a function of $V_g - V_{th}$ at 125 °C for peripheral PMOS transistors with L/W=2μm/10μm.

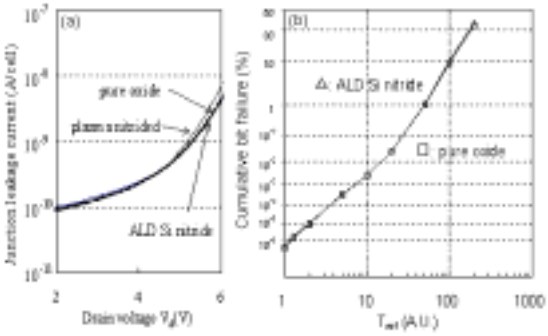

Figure 10 Memory-cell characteristics. (a) Junction leakage current of the transistors with the three kinds of gate dielectrics. (b)Data-retention characteristics of samples with the transistors having ALD stack gate dielectrics and pure gate oxide.

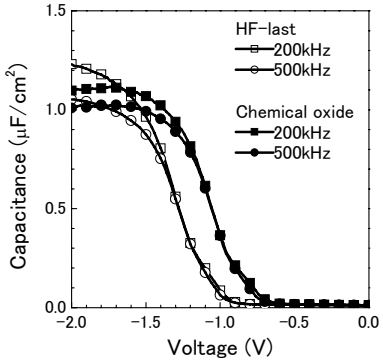

Figure 11 Capacitance-voltage curves measured at 200 and 500 kHz for Al/HfO_2/p-Si(100) (MIS) capacitors. The HfO_2 films were deposited by ALD on the bare Si and chemical oxidized Si for 40 cycles followed by PDA at 500℃ for 5 min in N_2 ambient.

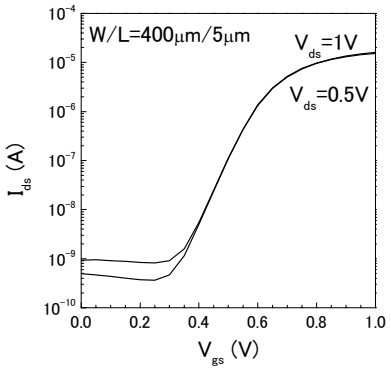

Figure 12 I_{ds}-V_{ds} characteristics of an NMOSFET with ~ 4 nm ALD HfO_2 gate dielectric and 200 nm Al gate electrode. L/W = 5μm/400μm, V_g from 0 to 1.0 V with a step of 0.25V.