An Object Detection/Recognition System using a 3-Dimensional Integration with Local and Global Wireless Interconnections

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1. Introduction

In order to realize hyper brain system which can recognize various objects in real-time/real-world, numbers of chips with massively parallel processing recognize various objects in real-time/real-world, numbers of chips with massively parallel processing and wideband interconnection capabilities are needed.

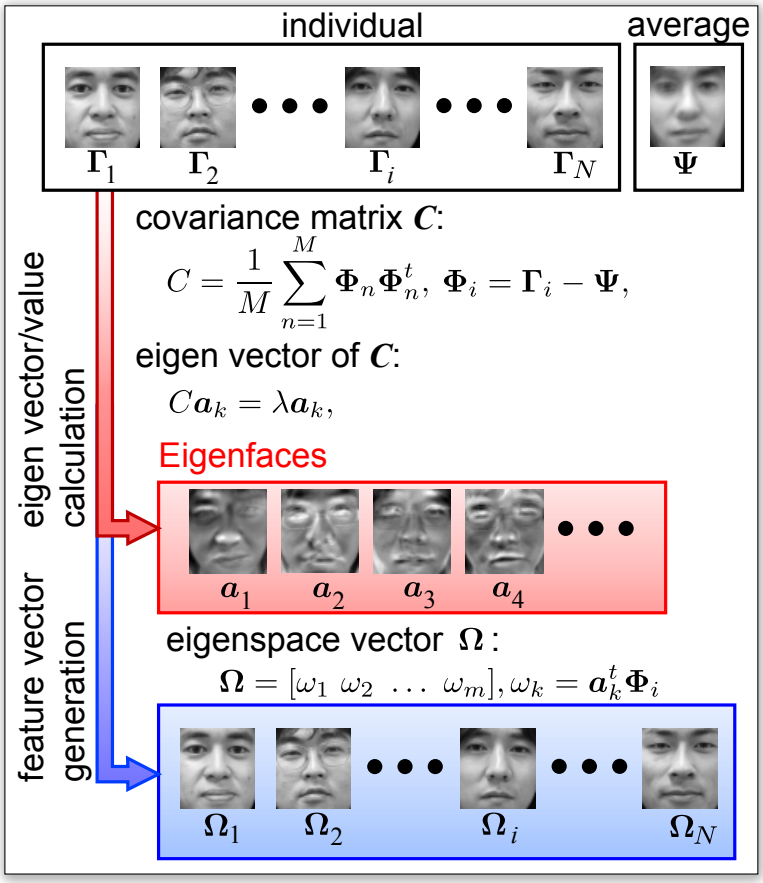
To solve the problem, we have proposed the 3-dimensional custom stack system (3DCSS) using two kinds of wireless interconnections: inductive coupling local wireless interconnect (LWI) and antenna coupling global wireless interconnect (GWI).

In this research, we have developed the architecture adopting Eigenfaces method based on PCA (Principal method with 3DCSS, we have proposed architecture of the multi-object recognition system. We have also types of chips with

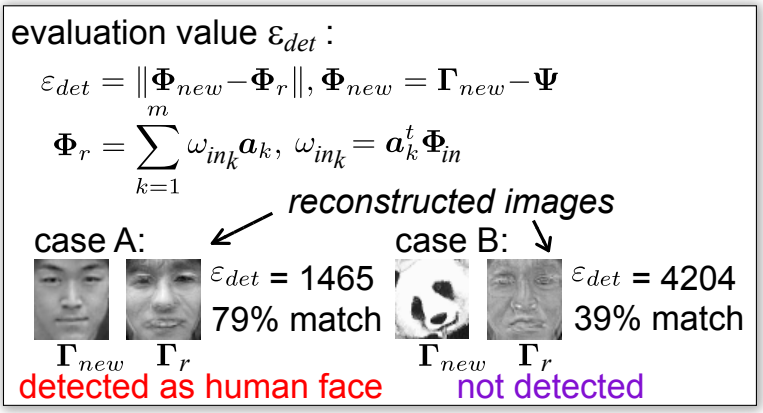
2. Object detection/recognition algorithm

The Eigenfaces method should be suitable for object recognition hardware architecture because of several advantages in both of recognition performance and hardware implementation. The various kinds of object can be detected and recognized by only preparing each individual database of them without changing processing. In hardware implementation, we can implement it with massively parallel circuit architecture and conventional digital circuit techniques without nonlinear processing, and design a chip which is nonlinear processing, and design a chip which is commonly applied to detection and recognition without increasing in circuit area.

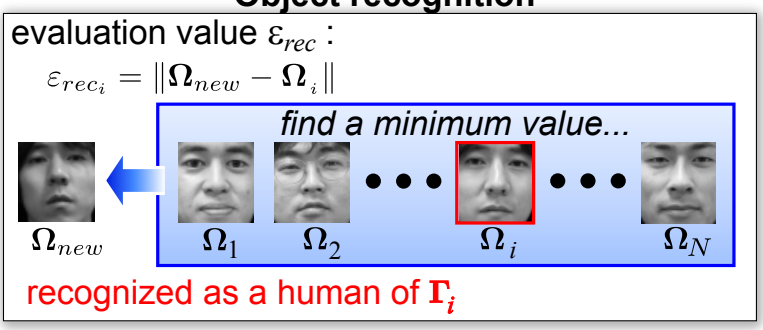
Object database



Object detection



Object recognition



3. Hardware implementation

The multi-object recognition system consists of three kinds of chips, that is Visual Processing chip (VP3D), Detection/Recognition chip (DR3D) and Reference Memory chip (RM3D). Each chip has 1x2ch LWIs which can transmit to and receive data from neighboring chips simultaneously and 2ch GWIs for clock and binary digital data receiving. The RM3D has 2ch GWIs and transmitter circuits for clock and data.

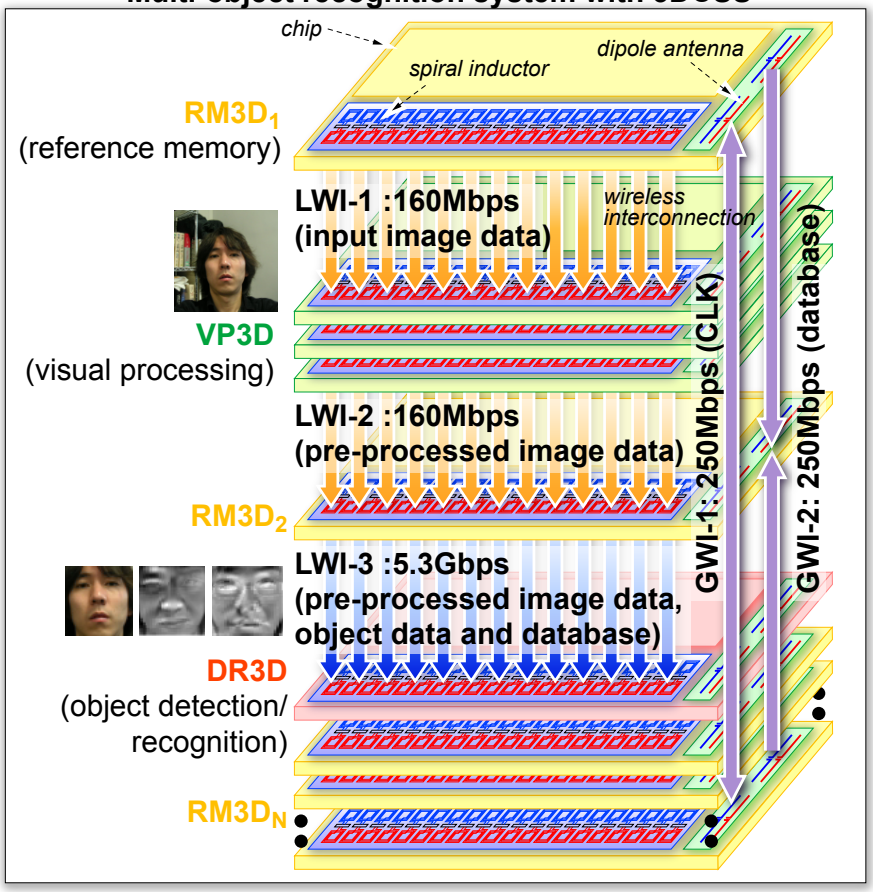
An original image data is stored in $RM3D_1$ and transmitted to neighboring VP3D in 21-pixel parallel PWM (pulse width modulation) signals (LWI-1). The massively parallel image pre-processing is implemented by several VP3Ds and resulted image data is transmitted to $RM3D_2$ with LWI-2 as same as LWI-1. The

DR3D receives processed image data and object database through LWI-3, or after storing other database to $RM3D_2$ from $RM3D_N$ by GWI-2, and detects and recognized objects.

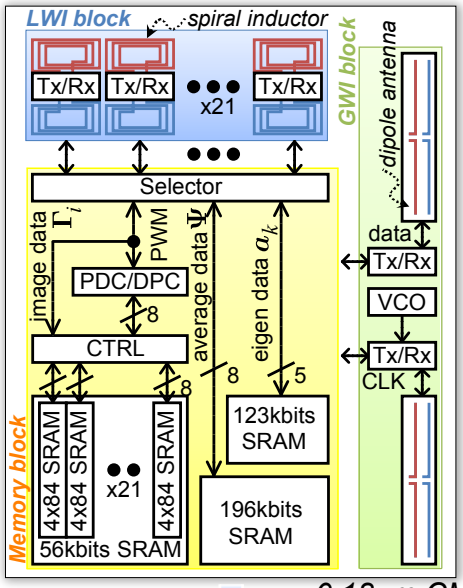
This system has the ability of 40GOPS (Giga Operation Per Second) at 250MHz operation.

Therefore, we expect to derive 160GOPS performance at the maximum LWI operation (1Gbps/1ch at present).

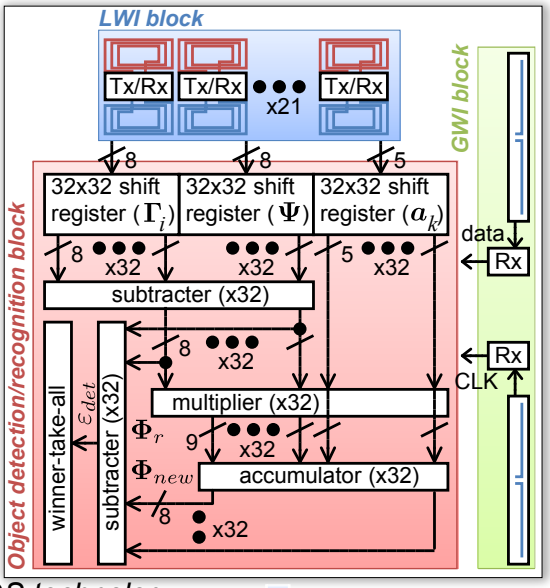
Multi-object recognition system with 3DCSS



Block diagrams of RM3D



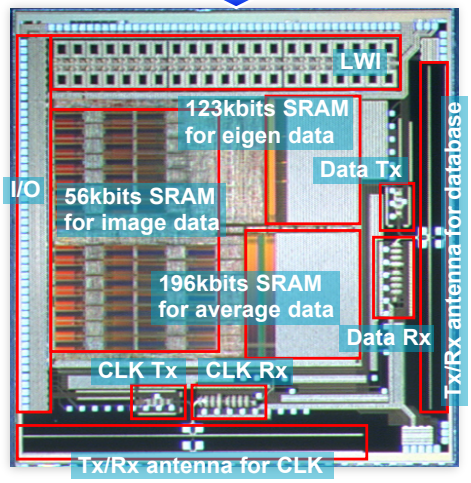
Block diagrams of DR3D



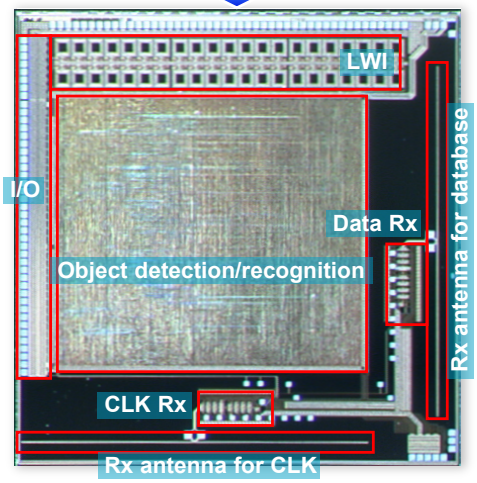
Specification

technology	0.18μm
supply voltage	1.8V
clock frequency	250MHz
chip size	5x5mm^2
image size	84x84
object size	32x32
RM3D	
image data	56kbits
average data	196kbits
eigen data	123kbits
DR3D	
detection time	580μs
recognition time (one-to-one)	4.2μs

0.18μm CMOS technology



Microphotograph of RM3D



Microphotograph of DR3D

The 20.6ms detection time and 12.7ms recognition time (30fps) should be achieved if we estimate the system ability at QVGA image which includes about 30 objects and 100 database objects.