A Vision System using a 3-Dimesional integration with Local and Global Wireless Interconnections

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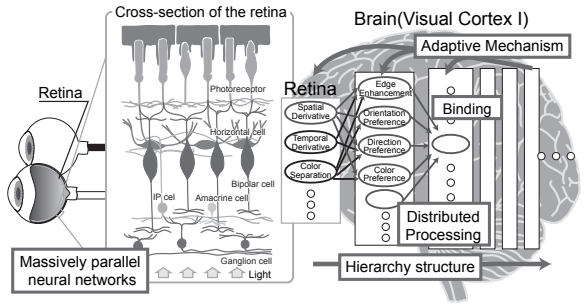
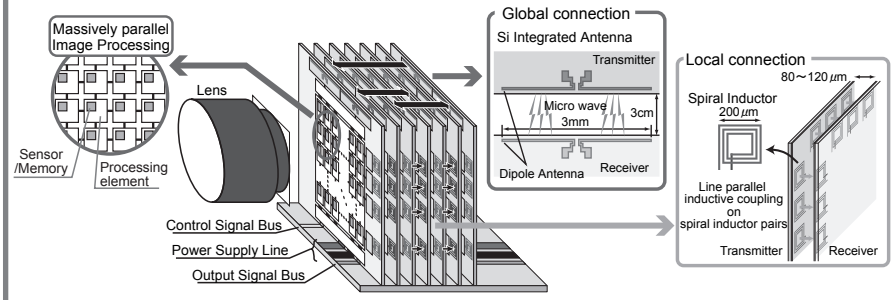
Vertebrate visual system



The vertebrate visual system processes visual information ***extraction*** and its ***binding*** by ***massively parallel*** neural network arranged ***hierarchically*** in ***real-time*** and ***adapts*** to a rapidly changing visual environment by an ***adaptive mechanism***.

Visual processing system using 3-Dimensional Custom-Stack System



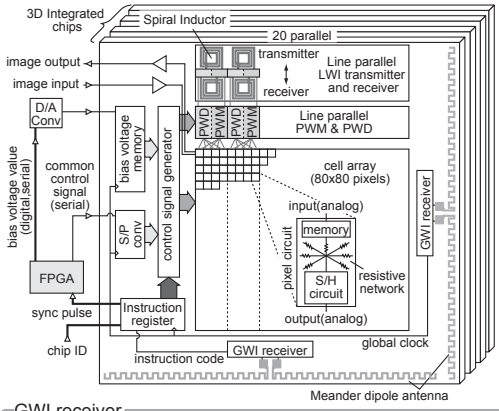
Power of the ***3-D integration*** is demonstrated by ***engineering realization*** of the ***architecture and algorithm*** of the vertebrate ***visual system***

Visual processing chip using the 3DCSS configuration with 0.35um CMOS process

A visual processing chip, a ***3VP3D chip***, was developed to configure the ***3DCSS***.

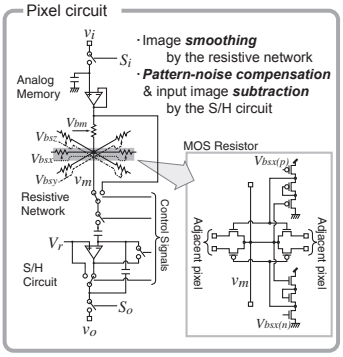
・Cell array : ***massively parallel image processing*** ・GWI circuit : ***global chip control*** by transmitting instruction code
・LWI circuits, PWM and PWD circuits : ***high speed data transfer*** by ***line parallel*** arrangement

Block diagram of the 3DCSS chip



The 3DCSS chip can be applied to processing mimicked ***vertebrate visual system*** due to the resistive network and the PWD circuit, etc.

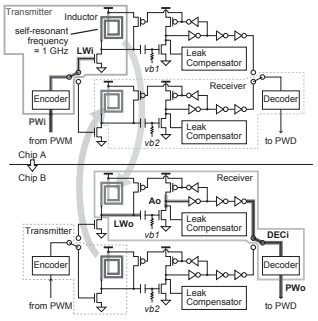
Pixel circuit



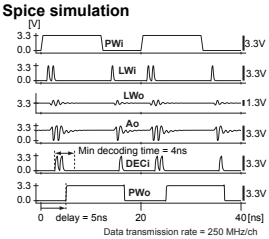
LWI transmitter and receiver

A pulse width signal from the pixel circuit is transferred from the ***LWI transmitter*** to the ***receiver*** between adjacent chips by using ***inductive coupling***. And then, the received signal is fed into the pixel circuit.

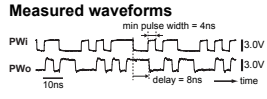
Block diagram of the LWI circuit



Spice simulation



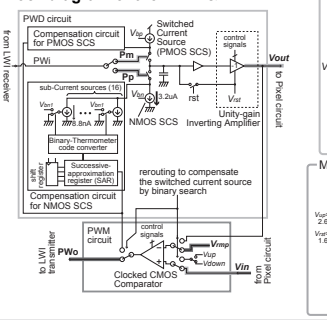
Measured waveforms



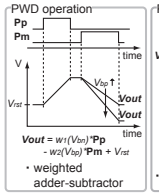
PWM and PWD circuits

An analog output from the cell array must be converted into a digital data in order to use the LWI circuits. The ***PWM*** circuit ***modulates*** the ***analog output*** to a ***pulse width*** signal, and the ***PWD*** circuit ***demodurates***. The PWM circuit was embedded a ***compensation circuit*** of the current source mismatches.

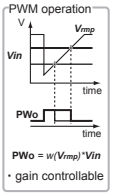
Block diagram of the PWM & PWD



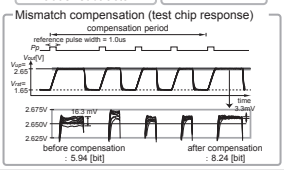
PWD operation



PWM operation



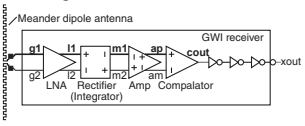
Mismatch compensation (test chip response)



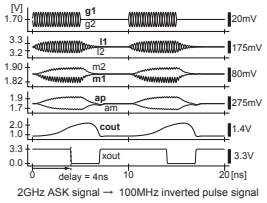
GWI receiver

The ***GWI receiver*** is used to get an ***instruction code***, which determines operations of each chip, for example, ***processing*** and ***transmitting methods***.

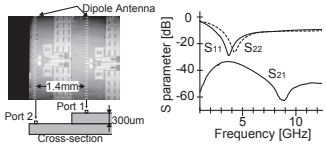
Block diagram of the GWI receiver



Spice simulation



Measured transmission characteristics of meander dipole antenna



Another circuits

Instruction register

An instruction code from a GWI receiver is fed into the instruction register in sync with a global clock from another GWI receiver. .

The register of each chip has unique ID number, and thus, can store a different instruction code.

Control signal generator

The generator generates control signals to the cell array, the PWM and the PWD circuits by combining the instruction code of each chip and common control signal, which generates an off-chip FPGA circuit.

Development of the 3DCSS test module

A 3DCSS test module using 3DCSS chip was developed by ultrasonic flip chip bonding process.

Cross section of the 3DCSS test module

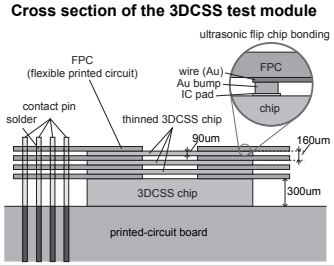
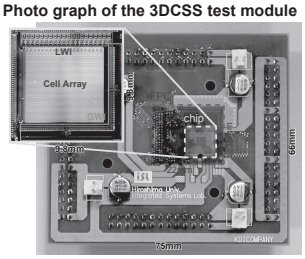
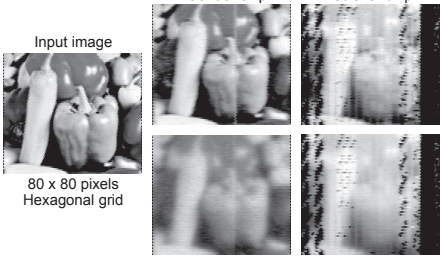


Photo graph of the 3DCSS test module



Responses obtained from the test module



An input image was fed into the sendor chip. The center images show outputs from the sendor chip. (upper : without smoothing, bottom : with smoothing) These images were transmitted to the receiver chip by using line parallel LWI circuits. The right images show output from the receiver chip.

The outputs had ***good transmitted parts*** and some ***incorrect parts***. If bias voltages of the LWI were changed the incorrect parts showed correct responses. The cause of this problem is thought that the ***distance between two spiral inductors*** of the test module had ***exceed the design value***.

Specifications of the VP3D chip

Process	CMOS 0.35um 2 Poly 3 Metal
Die size	9.8 x 9.8 [mm²]
Number of pixels	80(H) x 80(V) [pixel]
Number of LWIs	20 x 2 [cell] (transmitter and receiver)
Power supply	3.3 [V]

LWI transmitter & receiver circuit

Size	1100(H) x 400(V) [um²]
(Inductor)	(300(H) x 300(V) [um²])
Number of turns	6 (Top metal: 3, 2nd metal: 3)
Power consumption*2	5.6 [mW/cell] (transmitter + receiver)

PWM & PWD circuit

Size	332.4(H) x 344.8(V) [um²]
Resolution	8 [bit]
Power consumption*3	(PWM) 0.66 [mW/cell] (PWD) 1.70 [mW/cell]

GWI receiver circuit

Antenna length	8010 [um]
Size*1	858.1(H) x 820.0(V) [um²]
Power consumption	40 [mW]

Pixel circuit

Size	77.1(H) x 86.2(V) [um²]
Output accuracy*4	6~8 [bit]
Power consumption	(processing) 64.7 [uW/pixel] (readout) 78.9 [uW/pixel]

*1 Except antenna and wire areas.
*2 Pulse cycle = 2.0us, Pulse width = 1.0us.
*3 Maximum pulse width = 1.0us, Maximum voltage magnitude = 1.0V.
*4 Depend on an input image, a smoothing area of the resistive network, and etc.

Visual processing chip redeveloped with 0.18um CMOS process

To eliminate the problem in the visual processing chip developed with 0.35um CMOS process, a visual processing (re-VP3D) chip for 3DCSS was ***redeveloped with a 0.18um CMOS process***.

And then, a 3DCSS test module using the re-VP3D chips was redeveloped. ***The thickness of the thinned re-VP3D chip*** was about ***50um*** because the small die size makes thinning of the chip easier. Additionally, ***the thickness of the FPC and the height of the Au bump*** were reduced 30um and 20um, respectively. The distance between two spiral inductors was ***below the design value***.

Specifications of the re-VP3D chip

Process	CMOS 0.18um 1 Poly 6 Metal
Die size	5.0 x 5.0 [mm²]
Number of pixels	84(H) x 84(V) [pixel]
Number of LWIs	21 x 2 [cell] (transmitter and receiver)

LWI transmitter & receiver circuit

Size	552.8(H) x 190.0(V) [um²]
(Inductor)	(200.0(H) x 180.0(V) [um²])
Number of turns	9 (Top-3rd metal: 2, 2nd metal: 1)
Power consumption*2	1.59 [mW/cell] (transmitter + receiver)
Power supply	1.8 [V]

PWM & PWD circuit

Size	284.6(H) x 130.4(V) [um²]
Resolution	8 [bit]
Power consumption*3	262.6 [uW/cell] (PWM + PWD)
Power supply	1.8 [V]

GWI receiver circuit

Antenna length	3990 [um]
Size*1	872.9(H) x 409.6(V) [um²]
Power consumption	54 [mW]
Power supply	1.8 [V]

Pixel circuit

Size	32.6(H) x 29.1(V) [um²]
Output accuracy*4	6~8 [bit]
Power consumption	(processing) 81.5 [uW/pixel] (readout) 56.1 [uW/pixel]
Power supply	3.3 [V]

*1 Except antenna and wire areas.
*2 Pulse cycle = 1.5us, Pulse width = 1.0us.
*3 Maximum pulse width = 1.0us, Maximum voltage magnitude = 1.0V.
*4 Depend on an input image, a smoothing area of the resistive network, and etc.