Evaluation of Digital Crosstalk Noise to fully Differential VCO

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1. Introduction

With the progress of CMOS device scaling in mixed-signal LSIs, signal-to-noise ratio degradation of analog-circuits, which is caused by cross talk noise transferred from the digital circuits through silicon substrate, becomes a serious problem. The reduction techniques of this noise are key issues in RF and analog mixed LSI design.

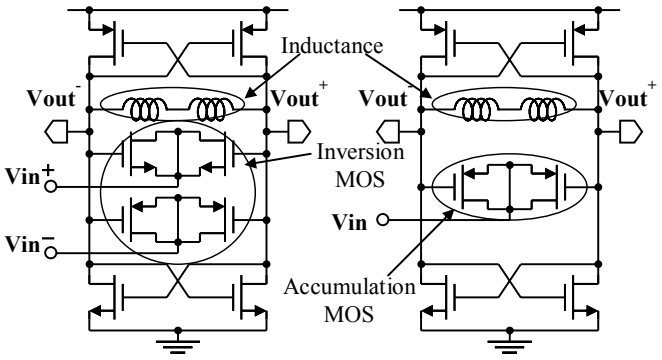
The purpose of this study is to measure and evaluate the effect of crosstalk noise on Voltage-Controlled Oscillators (VCOs), which are the most commonly used analog circuit in mixed signal LSI.

2. VCO

The VCO which generates a periodic signal is widely used as clock generation circuits for digital circuits and local oscillators of RF transceiver. The output frequency of VCO is controlled by the input voltage and its performance is evaluated by out put phase noise and jitter.

Performance Index: We evaluate phase noise of VCO as a performance index of frequency domain, and cycle-to-cycle jitter and cycle-jitter, as performance indices of time domain. The cycle-jitter is estimated from the histogram of period (T_i) in oscillation waveform, and, the cycle-to-cycle jitter is estimated by histograming the difference in periods from one cycle to the next (T_i-T_{i-1}). The cycle jitter is caused by low frequency component of noise and cycle-to-cycle jitter is caused by high frequency component. Each jitter was evaluated by the standard deviation (σ) and peak-to-peak (p-p) value.

Circuit configuration of VCO: A differential-input LC VCO using p- and n- inversion-MOS devices and single-input LC VCO using accumulation-MOS devices are shown in Fig. 1. Structures of the inversion and the accumulation devices are shown in Fig. 2. In the differential-input VCO, Two different control voltages around threshold voltages of n- and p-MOS are required. To solve the problem, the control voltages for n- and p-MOS are supplied through level shifting circuits. Even if the common mode input voltage changes, the total capacitance of the varactor is constant. Therefore, the differential-input VCO is insensitive to the change in common-mode of the control voltage.



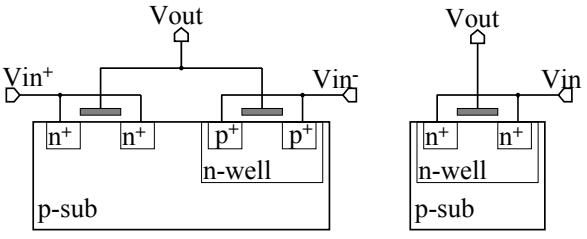
(a) Differential-input VCO (b) Single-input VCO

Fig. 1 Single and Differential-input VCO

3. Test chip design

To evaluate the influence of substrate noise to the VCO, well known controllable noise is generated in the substrate. As the noise source, transition controllable noise source (TCNS) was integrated on the chip. The noise wave form detector (NDET) is also integrated to measure substrate noise waveforms on the chip. [1,2] The TCNS has a nine-stage variable delay circuits which drive an array of 32 blocks of CMOS inverter arrays. When the delay set to minimum time 0.48nsec, the noise from each array is superimposed. The resulting noise waveform has one large peak at the transition time followed by a ringing waveform. The NDET measures the periodic noise waveform using the equivalent sampling technique. The input of the detector is connected to a probing point on the substrate contact or a GND wire. The voltage resolution and timing resolution of NDET is 100uV and 100ps, respectively.

The test chip, shown in Fig. 3, was fabricated in a 0.25um CMOS technology. To measure the influence of the substrate noise, the proposed differential-input VCO (VCO1), a conventional single-input VCO (VCO2) for comparison, two TCNSs, and NDETs are placed on the chip. The probes of NDETs can sense the potential changes of substrate near VCO and the GND line. The measured noises when the number of TCNS's active blocks is 64 are shown in Fig. 4.



(a) Inversion MOS (b)Accumulation MOS

Fig. 2 Structure of MOS varactor

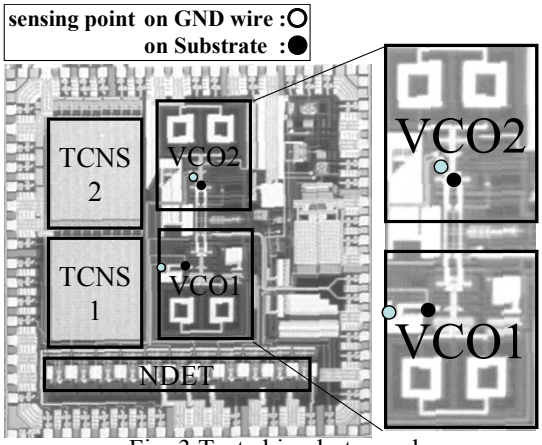
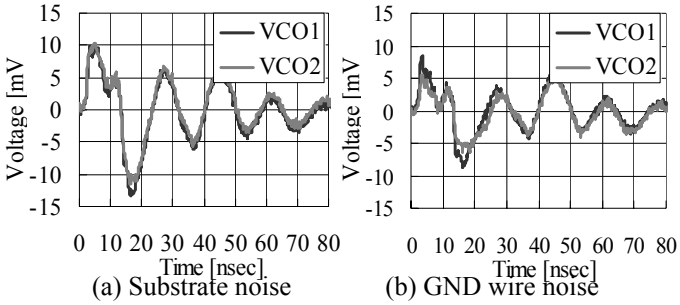
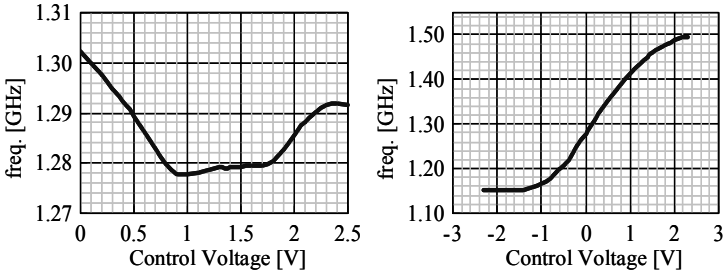


Fig. 3 Test chip photograph



(a) Substrate noise (b) GND wire noise

Fig. 4 Substrate and GND wire noises



(a) Vs common-mode input (b) Vs differential-mode input

Fig. 5 Measured f-V characteristics

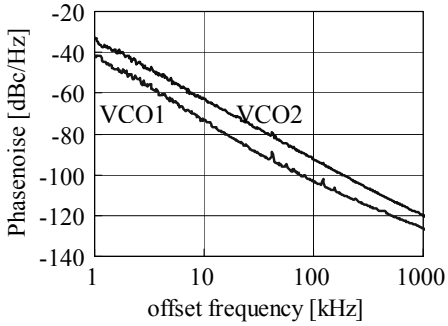
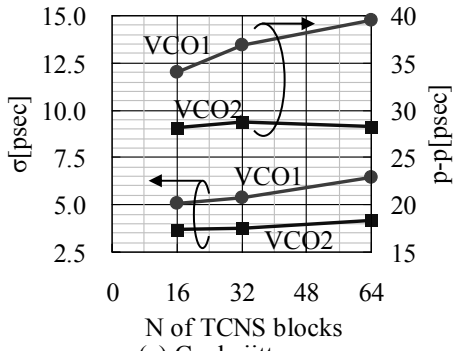
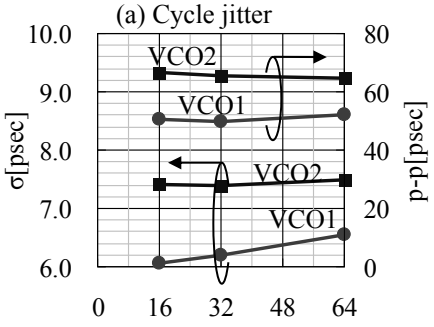


Fig. 6 Measured phase noise of VCO1 and VCO2



(a) Cycle jitter



(b) Cycle-to-cycle jitter

Fig. 7 Measured jitter vs the number of active TCNS blocks

Table1 Performance of VCO1 and VCO2

Performance index		VCO1	VCO2
Oscillation frequency[GHz]		1.28	1.54
VCO Gain[MHz/V]		147.6 (differential-mode input) / 0.7 (common-mode input)	145.3
Phasenoise@100kHz offset[dBc/Hz]		-104.0	-94.0
Cycle jitter [psec]	σ	3.00	2.59
	p-p	18.7	16.6
Cycle-to-cycle jitter[psec]	σ	4.21	5.07
	p-p	30.2	42.1

4. Measurement results

Frequency vs control voltage: Measured f-V characteristics of VCO1 are shown in Fig. 5, and the comparison between VCO1 and VCO2 is shown in Table 1. VCO1 has a gain of 147.6MHz/V for a differential-mode input voltage, and 700kHz/V for a common-mode input voltage. The VCO1 is robust to common-mode changes in the control voltage.

Phase noise and jitter: The phase noise characteristics are shown in Fig. 6. The phase noise of VCO1 at 100kHz offset frequency is improved by 10dB comparing with VCO2 which has the same VCO gain. When VCO1 compared with VCO2, the cycle-to-cycle jitter was improved by 20%, but cycle jitter was degraded.

Effect of cross talk noise: The output jitter of each VCO was measured to evaluate influence of substrate noise,

when the TCNS clock was 27MHz and the number of TCNS's active blocks was changed to be, 16, 32, and 64. The measured cycle jitter and cycle-to-cycle jitter are shown in Fig. 7. In all of the conditions, measured cycle jitter of VCO1 is over 10% large comparing with that of VCO2, but the cycle-to-cycle jitter is over 30% small. It indicates that VCO1 is affected by low frequency noise. The reason is considered as follows. The back-gate of n-inversion MOS directly connects to the substrate. On the contrary, p-MOS varactor is formed in the n-well which is connected to the substrate through a capacitance of pn junction. Thus low frequency substrate noise has large effect on VCO1. For high frequency noise, VCO1 is relatively insensitive and its jitter is lower than that for low frequency noise.

5. Conclusion

The differential-input VCO was designed using inversion-MOS as varactors. By the measurement of the test chip, we confirmed that it phase noise was improved by 10dB at 100kHz offset frequency, compared with the conventional single-input VCO. The effect of the substrate cross talk noise to the VCO jitter was also measured, using the on-chip noise source. The cycle-to-cycle jitter of the differential-input VCO was over 10% small comparing with the single-input VCO.

Acknowledgment

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