Development of Fabrication Processes for New SOI MOS Transistor and a Silicidation Technique for Source and Drain of Vertical Channel Devices

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1. Introduction

Three-dimensional (3-D) devices have been investigated for further scaled devices [1-2]. While, these devices have certain possibilities to realize various functions in future LSI. From this viewpoint, a new functional 3-D device has been developed and a silicidation technique of source and drain for 3-D structure devices has been investigated.

2. Development of a new SOI MOS transistor

Suppression of stand-by power is one of the key issues on VLSI circuits. Therefore, it has been studied to control the threshold voltage of MOSFET by various substrate biasing [3]. For a case of multi-gate devices, there is certain possibility to control device characteristics for respective device independently [4]. From this viewpoint, a narrow-channel SOI MOSFET with additional side-gate electrodes as shown in Fig. 1 is fabricated and investigated its subthreshold behavior [5].

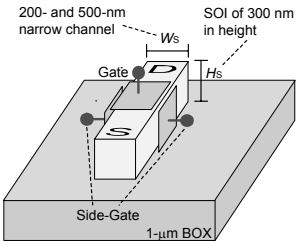


Fig. 1 A narrow-channel SOI MOSFET with additional gate electrodes. These gates are formed on both sides of an SOI channel.

A key fabrication process is shown in Fig. 2. After formation of SOI channel of 300 nm in height by RIE and deposition of poly-Si film, subsequent leveling is achieved by CMP. Gate electrode is formed on this surface and covered with its own thermal oxide. Additional side electrodes are delineated by RIE with SiO_2-covered gate as an etching mask.

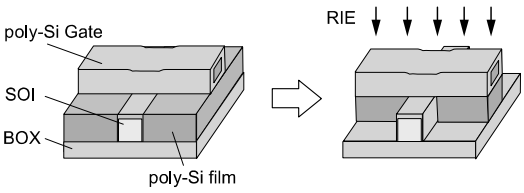


Fig. 2 A key fabrication process of the device. A gate electrode is formed on CMP etch-backed surface. Sidewall gates are formed subsequent RIE by using the top gate electrode as an etching mask.

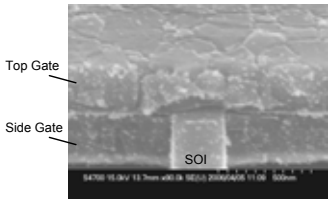


Fig. 3 An SEM image of fabricated gate structure. Additional-side-gate electrodes are successfully formed on both sides of the narrow SOI channel.

An SEM image for this structure is illustrated in Fig. 3. Subsequent source and drain formation is achieved by arsenic ion implantation and subsequent rapid thermal annealing. Gate oxide thicknesses are 4.7 nm for top one and 4.8 nm for additional side ones.

The device can be operated not only on fixed side gate biasing but also as tri-gate transistor shown in Fig. 4. I_D-V_G characteristics on these operations of devices with 190/330 and 480/280 in ratio of channel width and height, H_S/W_S are shown in Fig. 5.

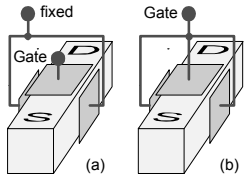


Fig. 4 Gate biasing modes of the device. Fixed side-gate biasing, (a) and tri-gate operation, (b).

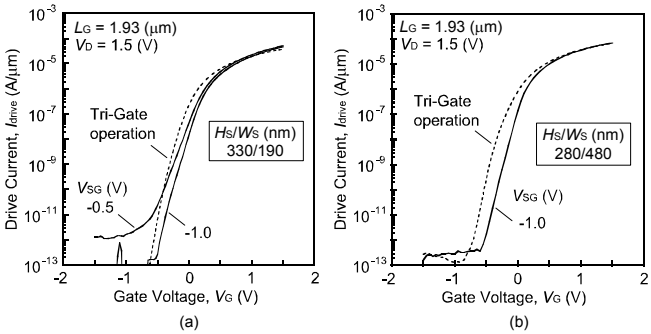


Fig. 5 Experimental I_D-V_G characteristics of the device. Improvement of subthreshold behavior by side-gate biasing and variation of threshold voltage are observed.

Improvement of subthreshold-current characteristics by side gate biasing and threshold-voltage variations between operation modes are observed. These are summarized in Fig. 6. An *S*-parameter is 79.8 mV/decade on tri-gate operation for both devices and varies from 95 to 150 mV/decade for fixed-V_{SG} operation. Threshold-voltage variation from that of tri-gate operation, ΔV_{TH} achieves 170 mV at V_{SG} = -1.0 V for both of devices though these *S*-parameters

are held at 95 and 117 mV/decade, respectively. Threshold-voltage variations are achieved in response to performance requirement.

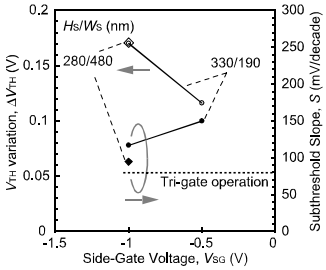


Fig. 6 Dependence of thereshold voltage and sub-threshold slope on side-gate biasing. V_{TH} is defined to be gate voltages at drive currents achieve at 100 nA/μm and ΔV_{TH} defined to be V_{TH} difference from that of tri-gate operation.

3. A silicidation technique for source and drain of vertical channel transistor

3-D transistors, e.g. FinFET, have been extensively developed for further scaled devices. While, beam-channel transistor, BCT with tall vertical Si channel shown in Fig. 7(b), have been developed aiming planer-area conscious driving current [6, 7]. Although, there are some issues because of its high-aspect-ratio structure.

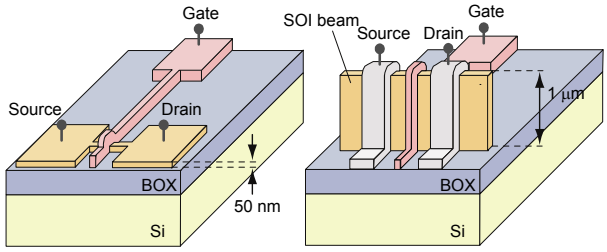


Fig. 7 FinFET and BCT developed in this study aiming planer-area conscious driving current.

Figure 8 shows simulated I_D-V_G characteristics of BCT with different two contact structures [8]. For tall vertical-channel transistors, usual top-contact structure causes decrease of driving current. Silicidation of source and drain provides a solution to this problem. From this viewpoint, silicidation process for vertical-channel device is investigated.

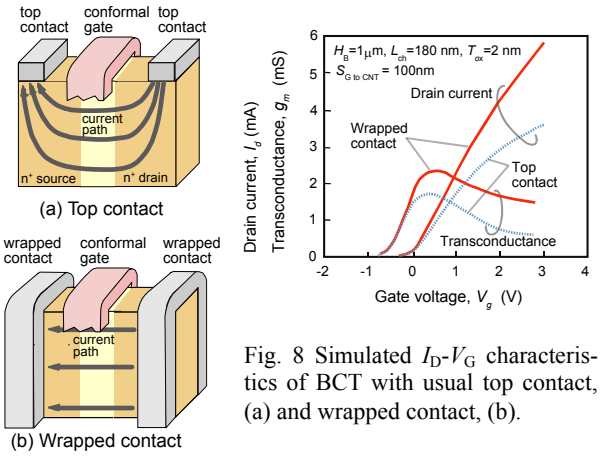


Fig. 8 Simulated I_D-V_G characteristics of BCT with usual top contact, (a) and wrapped contact, (b).

Process sequence is shown in Fig. 9. Beams having steep vertical walls are formed on (110) SOI using tetra-methl-ammonium-hydroxide, TMAH. Ni films are deposited by sputtering. Directionality of the sputtering causes deposition-rate difference between horizontal and vertical surfaces as shown in Fig. 10.

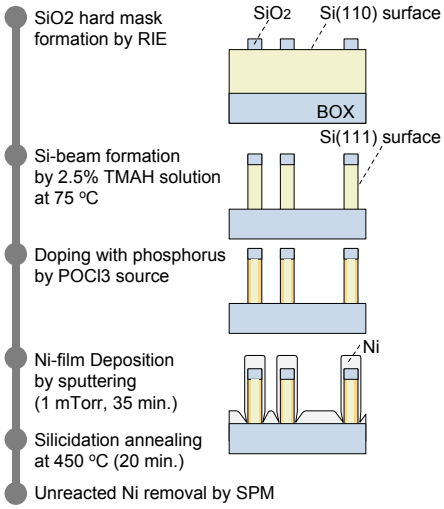


Fig. 9 Process sequence. Vertical walls are formed on (110) SOI using tetra-methl-ammonium-hydroxide, TMAH solution.

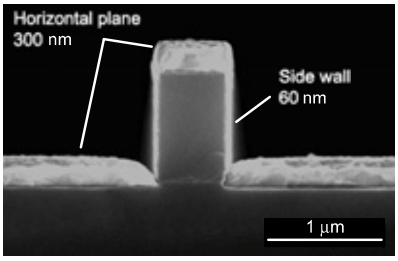


Fig. 10 An SEM image of deposited Ni film on vertical Si wall by sputtering method.

Silicidation annealing is implemented in deposition chamber at 450 °C. In this case, deformation of Si beams is observed as shown in Fig. 11. It is noted that wider beams are more deformed.

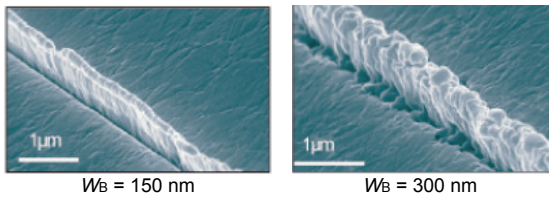


Fig. 11 Bird's eye views of Si beams silicided in deposition chamber at 450 °C.

To investigate its reaction mechanism, Ni film is deposited on SiO_2-patterned Si-substrate and is annealed 20 minutes at 450 °C. Ni-silicide film creeps up on SiO_2 as shown in Fig. 12. Its crept-up length from the edge of SiO_2 patterns is almost 2 μm although silicide film on Si-substrate is less than 500 nm in thickness [9].

From these results, it is understood that deformation of beams is caused by Si-diffused reaction to unreacted Ni-films on SiO_2. To avoid this, control of annealing condition is needed.

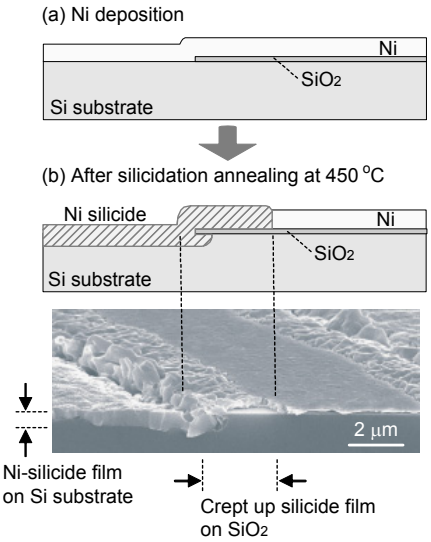
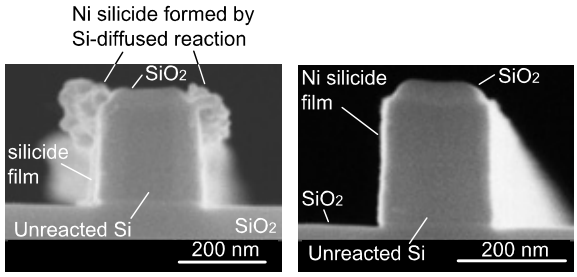


Fig. 12 Crept-up silicide on SiO_2 film. Its length from the edge of patterns is almost 2 μm.

Figure 13(a) shows an SEM image of a Si beam silicided by in-situ annealing at 300 °C. 55-nm-thick Ni-silicide film is formed on the sidewall, but silicide formed by Si-diffused reaction is observed. For the case of 250-°C annealing shown in Fig. 13(b), deformation caused by Si diffution is suppressed and 30-nm-thick silicide film is formed.



(a) 300 °C (b) 250 °C

Fig. 13 Silicided beams formed at 300 °C and 250 °C. In the former condition, Ni silicide formed by Si-diffused reaction is observed.

XRD spectrums for these samples are shown in Fig. 14. Ni_3Si_2 phase is observed as a dominant at 300-°C-annealing case, but deformation of Si-beam is occurred in this case. For 250-°C-annealing case, more Ni richer film, Ni_2Si phase is detected, and deformation of Si-beam caused by Si-diffused reaction is not observed. After annealing at 250 °C and unreacted Ni removal by SPM, NiSi film is obtained by rapid thermal anneling at 450 or 500 °C avoiding Si-beam deformation.

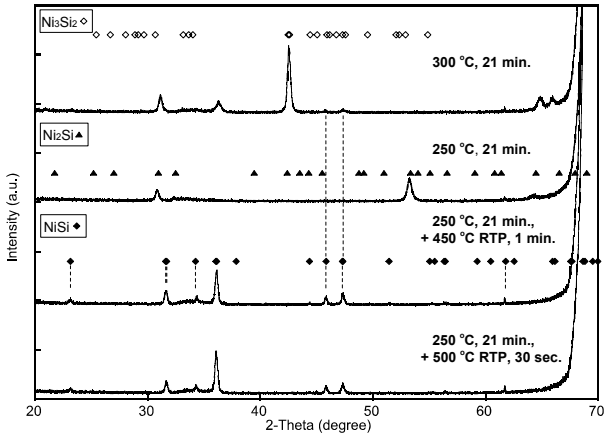


Fig. 14 XRD spectrums of silicided samples annealing at 300 and 250 °C and 2-step annealing.

Figure 15 shows an SEM image of a silicided beam by 2-step annealing process. 60-nm-thick NiSi film is uniformly formed on the sidewall without abnormal deformation of Si-beams.

A silicidation process for vertical structure device is discussed. For cases of annealing at 300 °C or more, Si-diffused reaction causes deformation of beams. 2-step annealing process prevents this phenomenon and NiSi film is successfully formed on vertical walls.

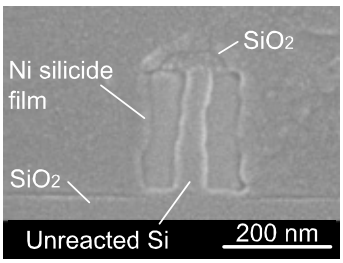


Fig. 15 A cross-sectional view of Ni-silicided beam formed by 2-step annealing process.

4. Summary

In this paper, development of a new functional 3-D device and a silicidation technique of source and drain for 3-D structure devices have been discussed.

An SOI nMOSFET with additional side gate electrodes is fabricated and discussed its subthreshold behaviors. Threshold-voltage variations are achieved in response to performance requirement. In the viewpoint of stand-by-power suppression, these provide certain controllability to circuit operation.

In the silicidation process for vertical structure device, Si-diffused reaction causes deformation of Si-beams in cases of annealing at 300 °C or more. A 2-step annealing process prevents this phenomenon and NiSi film is successfully formed on vertical walls.

Acknowledgements

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