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Development of Fabrication Processes for New SOI MOS Transistor and a Silicidation Technique for Source and Drain of Vertical Channel Devices

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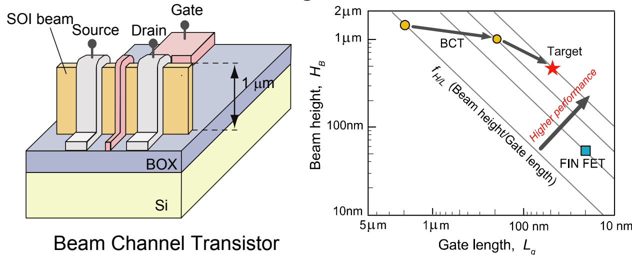
Introduction

Three-dimensional (3-D) devices have been investigated for further scaled devices. While, these devices have a certain possibilities to realize various functions in future LSI.

- Beam Channel transistor

Planer-area conscious driving current



Beam Channel Transistor

From this viewpoint, a new functional 3-D device has been developed and a silicidation technique of source and drain for 3-D structure devices has been investigated.

Contents:

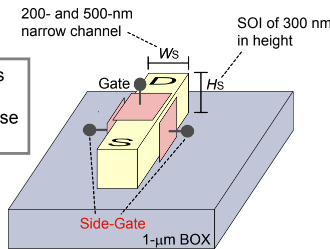
A. Developement of a new SOI MOS transistor

B. A silicidation technique for source and drain of vertical channel transistor

A. Developement of a new SOI MOS transistor

Suppression of stand-by power is one of key issues on VLSI's. Therefore, it has been studied to control the threshold voltage of MOS transistor by various substrate biasing.

For a case of multi-gate device, there is certain possibility to control its device characteristics independently using these gates.



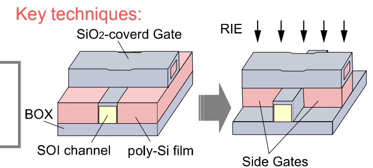
A narrow-channel SOI device with additional side gate is fabricated and its subthreshold behaviors are discussed.

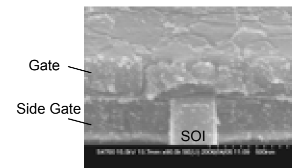
Device Fabrication

Formation of electrically separated electrodes on top and side regions of SOI channel is needed.

A technique utilized top gate as an etching mask for side electrode formation

Key techniques:



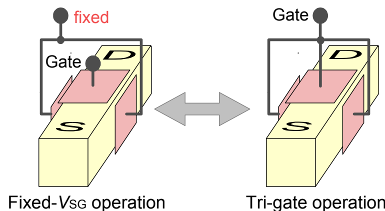


Additional side gate electrodes are successfully formed on both sides of the narrow SOI channel.

Experimental Results

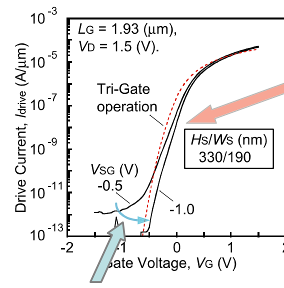
The device provides some operation modes using electrically separated gates.

Device-characteristics variation through these operation modes and effects of V_{SG} are discussed.



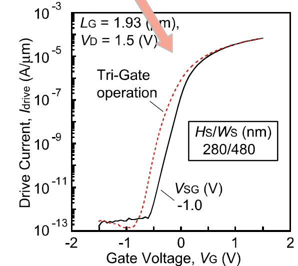
Fixed-V_{SG} operation   Tri-gate operation

I_D-V_G characteristics



Threshold-voltage variation

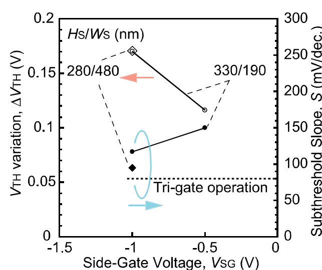
Improvement of Subthreshold behavior



T_{OX}: 4.7 nm (top gate), 4.8 nm (side gates).

V_{TH}-variation and S-parameter

Threshold-voltage variation, ΔV_{TH} is defined to be deference from that of tri-gate operation.



V_{TH} = V_G@I_{drive} = 100 (nA/µm)

ΔV_{TH} achieves 170 mV for both of devices.

	ΔV_{TH} (mV)	S-parameter (mV/dec.)
Tri-gate operation		79.8
V_{SG} = -1.0 V, H_S/W_S = 330/190	170	95
V_{SG} = -1.0 V, H_S/W_S = 280/480	171	117

S-parameters are held at 95 and 117 mV/decade.

An SOI nMOSFET with additional side gate electrodes is fabricated and discussed its subthreshold behaviors.

Device Fabrication:

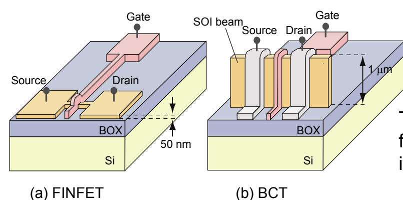
Formation of electrically separated electrodes. → A self-aligned technique utilized top gate as an etching mask for side electrodes formation is adopted.

Device Characteristics:

Threshold-voltage variations are observed by choosing rather small additional-gate voltage. These sensitive responses to side-gate biasing can be realized because of its thin gate oxide.

B. A silicidation technique for source and drain of vertical channel transistor

3-D transistors, e.g. FinFET, have been extensively developed for further scaled devices. While, beam-channel transistor, BCT with tall vertical Si channel have been developed aiming planer-area conscious driving current.



(a) FINFET (b) BCT

There are some issues on fabrication process because of its high-aspect-ratio structure.

- Patterning of high-aspect-ratio Si channel
- Doping to sidewall of vertical channel

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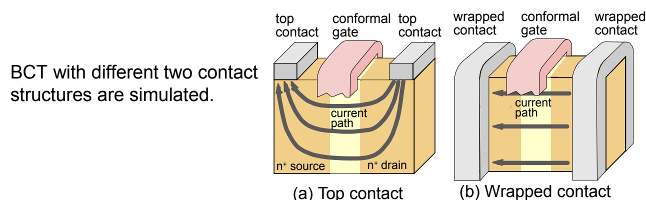
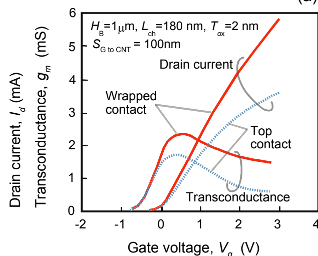
Importance of low resistive source and drain for BCT

BCT with different two contact structures are simulated.



(a) Top contact (b) Wrapped contact



For tall vertical-channel transistors, usual top-contact structure causes decrease of driving current.

Silicidation of source and drain provides a solution to this problem.

Experimental

- SiO_2 hard mask formation by RIE
- Si-beam formation by 2.5% TMAH solution at 75 °C
- Doping with phosphorus by $POCl_3$ source
- Ni-film Deposition by sputtering (1 mTorr, 35 min.)
- Silicidation annealing at 450 °C (20 min.)
- Unreacted Ni removal by SPM

SiO_2 Si(110) surface BOX Si(111) surface Ni

Directionality of the sputtering causes deposition-rate difference between horizontal and vertical surfaces.

Silicidation annealing

W_B = 150 nm W_B = 300 nm

Deformation of Si beams is observed. It is noted that wider beams are more deformed.

Si-diffused reaction to unreacted Ni film

To investigate its reaction mechanism, Ni film is deposited on SiO2-patterned Si-substrate and is annealed 20 minutes at 450 °C.

(a) Ni deposition

(b) After silicidation annealing at 450 °C

Ni silicide, Ni, SiO_2, Si substrate, 2 μm

Ni-silicide film on Si substrate

Crept up silicide film on SiO_2

Deformation of beams is caused by Si-diffused reaction to unreacted Ni films on SiO_2. To avoid this, control of annealing condition is needed.

Crept-up length	: 2 μm
Silicide film on Si	:500 nm

2-step annealing process

1st annealing in deposition chamber

300 °C — Ni silicide formed by Si-diffused reaction; SiO_2; silicide film; Unreacted Si; 200 nm

250 °C — Ni silicide film; SiO_2; Unreacted Si; 200 nm

Deformation caused by Si diffution is suppressed.

2nd annealing by RTP at 450 °C

Ni silicide film; SiO_2; Unreacted Si; 200 nm

Ni_3Si_2 ◇, Ni_2Si ▲, NiSi ●; 300 °C, 21 min.; 250 °C, 21 min.; 250 °C, 21 min., + 450 °C RTP, 1 min.; 250 °C, 21 min., + 500 °C RTP, 30 sec.; Intensity (a.u.); 2-Theta (degree)

60-nm-thick NiSi film is uniformly formed on the sidewall without abnormal deformation of Si-beams.

For tall vertical-channel transistors, usual top-contact structure causes decrease of driving current. Silicidation of source and drain provides a solution to this problem.

From this viewpoint, silicidation process for vertical-channel device is investigated.

For cases of annealing at 300 °C or more, Si-diffused reaction causes deformation of beams.

2-step annealing process prevents this phenomenon and NiSi film is successfully formed on vertical walls.

Summary

Development of a new functional 3-D device and a silicidation technique of source and drain for 3-D structure devices have been discussed.

- An SOI nMOSFET with additional side gate electrodes is fabricated and discussed its subthreshold behaviors. Threshold-voltage variations are achieved in response to performance requirement. In the viewpoint of stand-by-power suppression, these provide certain controllability to circuit operation.
- In the silicidation process for vertical structure device, Si-diffused reaction causes deformation of Si-beams in cases of annealing at 300 °C or more. A 2-step annealing process prevents this phenomenon and NiSi film is successfully formed on vertical walls.