Application of Fully Parallel Associative Memory in Two-Stage Pattern Matching

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1. Introduction

Associative memories have been studied and used as a possible solution for speeding up time-consuming content related searches and for allowing access to data by name or partial content rather than by location or address. Content addressable memory based associative processors are proposed for different applications such as pattern recognition, data compression and intelligent processing to reduce the considerable amount of memory accesses and processing time. Fully-parallel solution employing Hamming distance [1] is initially used for associative processing since it can be realized by less computational effort. On the other hand, Manhattan distance [2] and Euclidean distance [3] based associative processors are capable of many practical applications such as vector-quantization recognition, code-book-based image compression and so on. But all these architectures are based on single winner search and applicable only for single stage recognition systems. So, the reliability of these systems is low for different applications.

In this paper, a mixed digital-analog cascaded associative memory based system with two-stage winner search is proposed. In the first stage, winner search is done in sequential order to find not only the best nearest-match data but also a freely chosable number of *k* nearest-matches from the main reference data. Then, in the second stage, the winner is searched in the additional feature memory among the *k*-nearest-matched rows, determined by the first associative memory, to get the final winner.

2. Cascaded Associative Memory Architecture

A block diagram of the proposed cascaded associative memory architecture is shown in Fig.1. It contains two associative memory blocks, one for the main reference data and another for the additional feature reference data. The first associative memory part shown in Fig. 2 is designed in a way that it can search *k*-nearest-matches. The value of *k* can be selected according to the user's wish. The memory part consists of conventional read/write periphery for storing the reference-data words and for reading out the nearest-match data. A row of the memory field contains *W* storage cells (SC), each with *n* bits plus the circuitry for unit comparison (UC) and word comparison (WC). The unit comparators use digital circuits for subtraction and absolute value calculation. The digital outputs of the absolute unit distance values are then converted into analog currents using the current converters (CC). In case of the Euclidean distance the analog currents from each *CC* are then squared using analog current squarer circuits. Finally, the output currents from all squarer circuits are added to get a Euclidean-distance-equivalent current which constitutes the match line current. The word-comparison results C_i are transferred to the winner-search circuit consisting of the winner-line-up amplifier (WLA) and the winner-take-all circuit (WTA). The closely coupled interaction of *WLA* and *WC*s makes it possible to achieve desired maximum amplification of winner-loser distances for all search cases. The functionality of *WLA* is to pre-amplify the match lines and restrict the large variety of possible analog outputs to a small range by self-regulation. The *WLA* amplifies the differences of current signals between winner and losers and regulates the winner signal to a suitable level for further distance amplification. The results are then fed to a *WTA* network for recognizing the winner and losers precisely. In the nearest match search block, the functionality of the *WTA* circuit is to further amplify the winner-loser distances by voltage-current-voltage transformations and provide a further strong amplification of the winner-loser differences. Final decision circuits, consisting of inverters with an adjusted switching threshold, are connected after the *WTA*, and generate a "1" for the winner row and a "0" for each loser row. Finally, from the output of each *WTA* one feedback line is added to the corresponding match line through a feedback element. It forces the previous winner line to become a loser when the enable signal is raised again. The layout in Fig. 3 shows the designed associative memory for *k*-nearest-matches search, which measures 5.12 mm^2 in 0.35μm, 2-poly, 3-metal CMOS technology. It contains 64 reference words with 16 binaries each 5-bit long. Figure 4 shows the simulation result from the layout extracted netlist. Here the search result up to fourth-nearest match or fourth winner is shown. The input-winner distances (Euclidean) of the reference patterns are 1, 2, 3, and 4, respectively.

To connect the second associative memory with the first one we have added a multiplexer before the row decoder. It initially provides addresses to store the feature reference data in the memory and during the search operation it provides the address of the *k*-nearest-matched lines selected by the first associative memory to activate these lines for final winner search in second stage. The second associative memory contains some characteristic feature data of the input pattern stored in the first associative memory. The features are selected in such a way that they have the minimum dependency on size and variation of data. Given a segmented character we have extracted its moment based features as follows [4]: *Total mass* (number of pixels in a binarized character), *Centroid*, *Elliptical parameters* (i.e. *Eccentricity* (ratio of major to minor axis) and *Orientation* (angle of major axis)), and *Skewness*. The second associative memory can be an ordinary type to search only one winner or can be similar to the first associative memory which can search the final winners in sorted form.

3. Simulation Results

We have examined the system performance in a real application for hand written English character recognition using MATLAB software. A number of 35 datasets of English characters written by four different writers were

used for the experiment. Figure 5 shows some gathered data samples. We have tested our proposed system and compared the results with a system which uses only one associative memory. The results are shown in tabular form in Table I. From the table we can see that the proposed system has improved the reliability of pattern matching and the misclassification rate is reduced from 13% to 5.3%.

4. Conclusion

A cascaded fully parallel associative memory with two-stage winner search is proposed. It significantly improves the reliability of a object recognition system as we have seen from Table I. Since both associative memories can be used for different distance measures, it is possible to implement a hybrid distance measures in the two-stage pattern matching system.

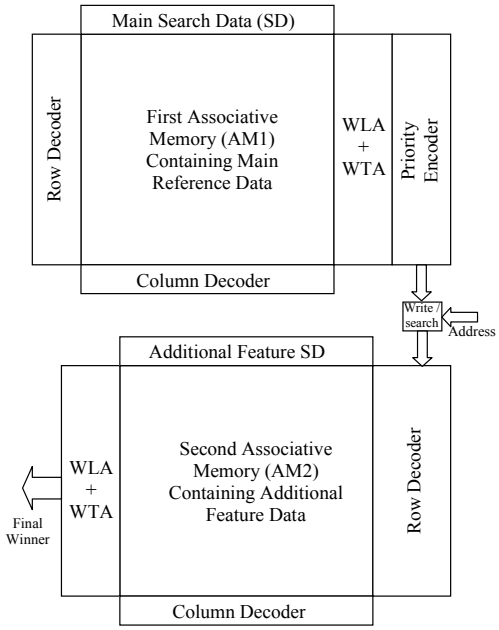

Fig. 1 Block diagram of the two-stage winner search system.

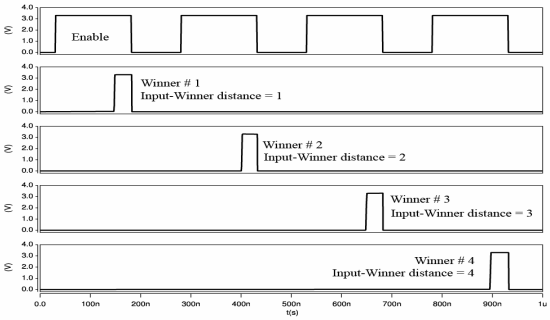

Fig. 4 Simulation result from layout extracted netlist.

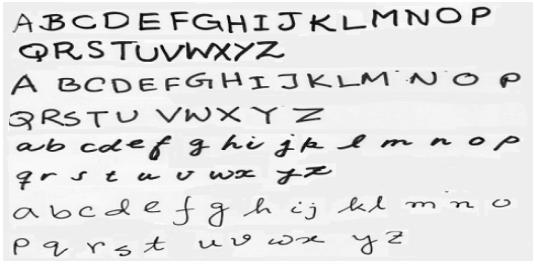

Fig. 5 Handwritten samples from different writers used as input data.

Acknowledgement

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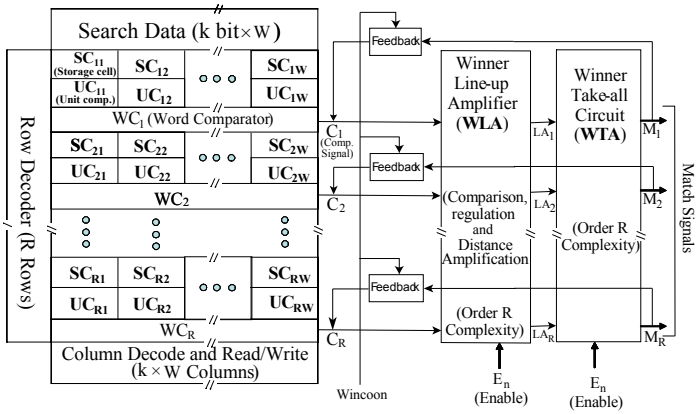

Fig. 2 Block diagram of the fully-parallel associative memory for k-nearest-matches search.

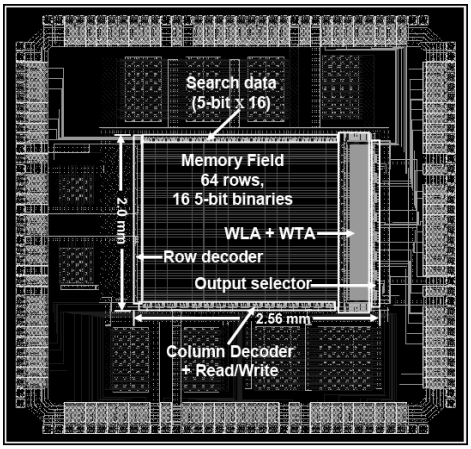

Fig. 3 Layout of the associative memory for k-nearest-matches search.

Table I
Classification results for two datasets from different writers

Writer	**Test Set 1** (26 samples)		**Test Set 2** (26 samples)	
	Miss-classify		Miss-classify	
	Single-stage	Two-stage	Single-stage	Two-stage
A	4	2	4	2
B	4	1	3	1
C	3	1	3	1
D	2	1	4	2
Total	12.5%	4.8%	13.5%	5.8%