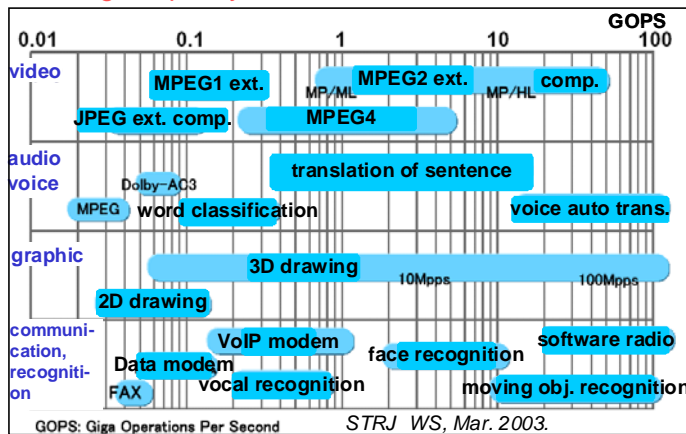


# Highly-parallel Table-Lookup-Coding with Scalable Architecture using Flexible Multi-Ported Content Addressable Memory

Takeshi Kumaki, Yutaka Kono, Masakatsu Ishizaki, Tetsushi Koide and Hans Jürgen Mattausch  
Research Center for Nanodevices and Systems, Hiroshima University

## Background & Motivation

End-user can readily make use of **high quality** and **high capacity** multimedia data.



required performance of a multimedia LSI

## For Fast Processing

◆ **Repeated operation**: arithmetic-logic operations carried out for all data.

parallel processing

◆ **Table-lookup-coding**: coding operation using a code word table  
Reading from SRAM and comparing  
Coding by CAM or hard-wired logic

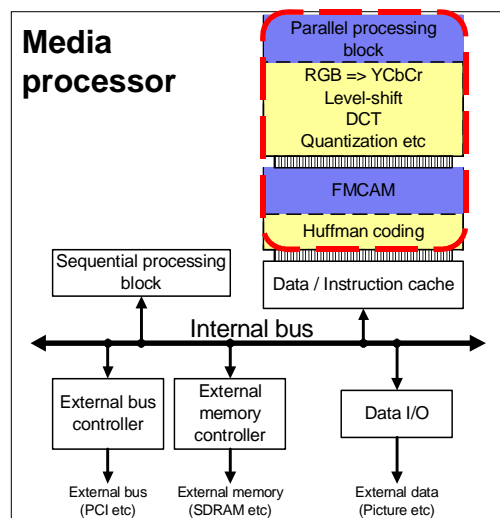
Efficient parallel processing is difficult

Realizing the parallel Huffman encoding

## Architecture Concept

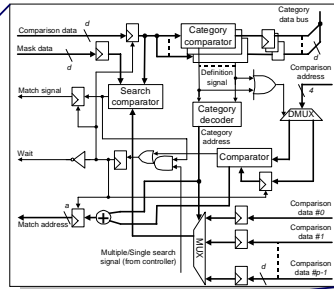
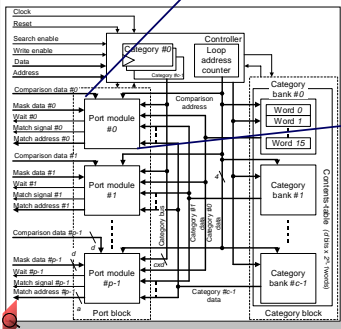
- ◆ Combining parallel and sequential processing blocks  
→ Decreases the frequency of bus conflicts

- Saving processing time
- Small area and low power consumption



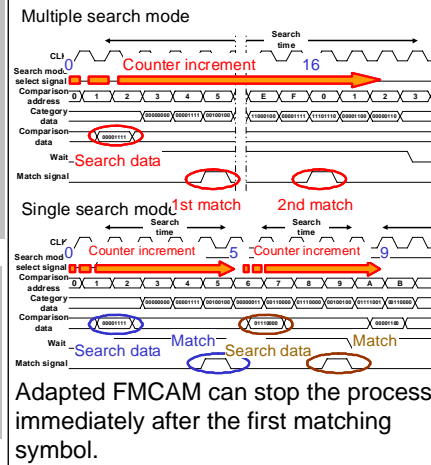
## Adapted Flexible Multi-ported CAM (FMCAM)

- ◆ Bit-Parallel and Block-Parallel (BPBP) search
- ◆ Categorization of the stored reference words
- ◆ P input/output



- ◆ Asynchronous processing at each port
- ◆ Multiple/Single search mode
- ◆ Counting value setting mode

### Multiple/Single search mode waveform

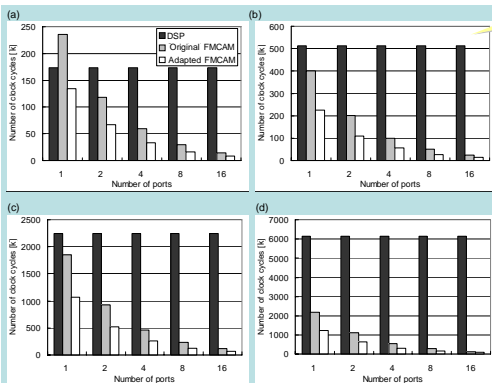


## Implementation results for JPEG Application

(a) 154 x 144 (b) 256 x 256 (c) 600 x 480 (d) 1024 x 768



Adapted FMCAM processing clock cycles are **43% less** than for original FMCAM and **93% less** than for DSP



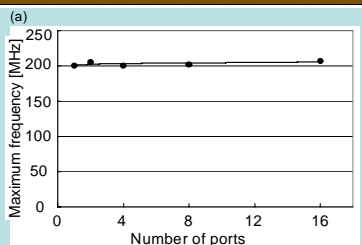
Comparison of clock cycles for Huffman encoding

### Comparison of Processing Efficiency

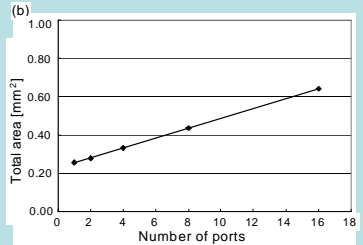
Ports	Maximum frequency		Comparison operation (MOPS)			Total area [mm <sup>2</sup> ]		MOPS / mm <sup>2</sup>		
	Original Adapted FMCAM	Parallel DSPs	Original FMCAM	Adapted FMCAM	Parallel DSPs	Original Adapted FMCAM	Parallel DSPs	Original FMCAM	Adapted FMCAM	Parallel DSPs
1	200	200	10.55	18.58	25.60	0.26	0.21	41	72	122
2	205	200	21.61	38.11	51.20	0.28	0.42	78	137	122
4	201	200	42.26	74.61	102.40	0.33	0.84	127	224	122
8	202	200	85.18	149.14	204.80	0.44	1.68	195	342	122
16	207	200	174.11	302.92	409.60	0.64	3.36	271	472	122

Performance per area size of adapted FMCAM is **1.7 times** higher than for original FMCAM and **3.8 times** higher than for DSPs. (for 16 ports)

## Implementation Result



Maximum operating frequency is practically not influenced by the number of ports.



The area increases only linearly with just about 9% per port. Synthesized with the Synopsys Design Compiler for 90nm CMOS technology

## Conclusion

- ◆ Multi-ported CAM for parallel coding is proposed as a novel architecture for table-lookup-coding.
- ◆ In the JPEG application, the clock cycle number of the adapted FMCAM is **up to 93% smaller** than for a conventional DSP.
- ◆ The efficiency of the adapted FMCAM in MOPS/mm<sup>2</sup> is **up to 3.8 times higher** than that of conventional parallel operated DSPs.