Circuit Design of a Single-chip Ultra-Wideband Receiver using Silicon Integrated Antennas

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UWB Receiver

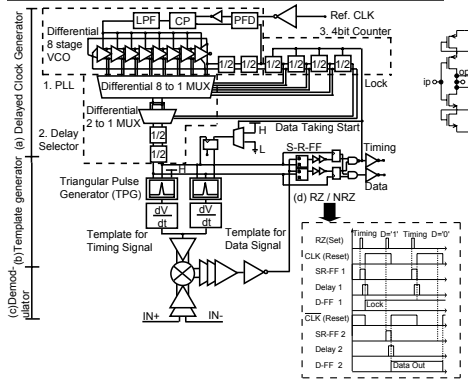
Synchronization and Data Acquisition

•Synchronous pulse detection by taking a correlation between the received signal and template is important.
•The received signal has alternately coming timing pulse and data pulse. The time difference between timing pulse and data pulse is a 50% of the cycle of the clock.
•Receiver generates double GMP templates. 1st template is used for the detection of the timing pulse, and 2nd template is used for the detection of data pulse.

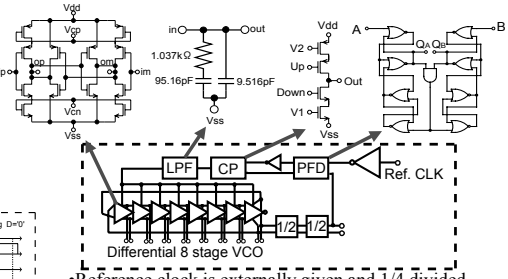
Circuit Blocks

UWB receiver is composed of 4 blocks.
(a) Delayed clock generator
(b) Template generator
(c) Demodulator
(d) Return Zero (RZ) / Non Return Zero converter

Block Diagram

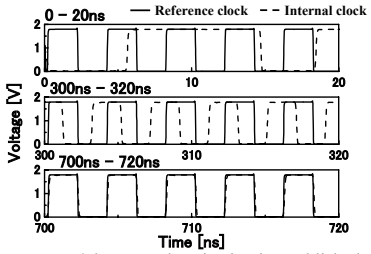


Phase-Locked Loop (PLL)



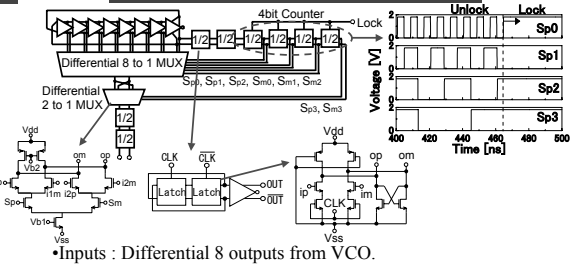
•Reference clock is externally given and 1/4 divided internal clock is compared to reference clock.
•PLL performs frequency and phase synchronization between reference clock and internal clock.

Simulation Results of PLL



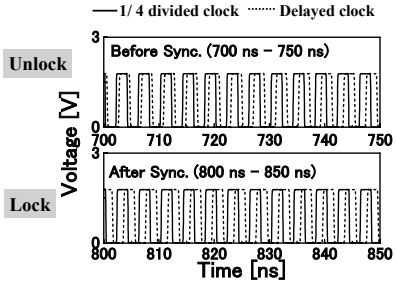
• Frequency/Phase synchronization is established between reference clock and 1 /4 divided internal clock.

Delayed Clock Generation

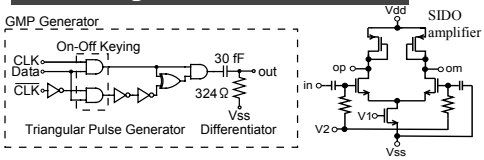


•Inputs : Differential 8 outputs from VCO.
•Output: Differential, sequentially delayed and 1 /4 divided clock.
•Control signals: S_{p0},S_{m0} ~ S_{p3}, S_{m3} comes from 4 bit counter.

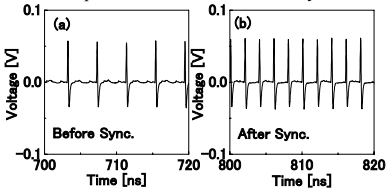
Delayed Clock



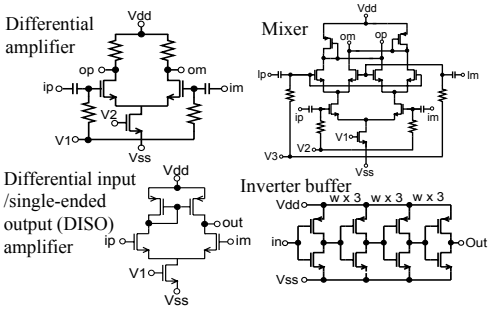
Template Generator



Double GMP template generators
1st: Timing pulse detection → Always On
2nd: Data pulse detection → On After synchronization



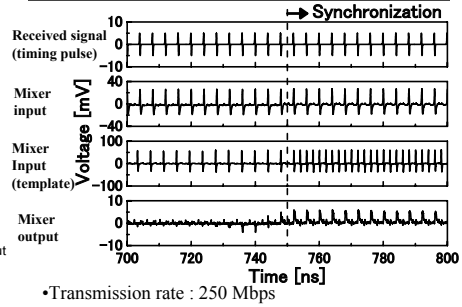
Demodulation Circuits



• Mixer multiplies the received signal by template.

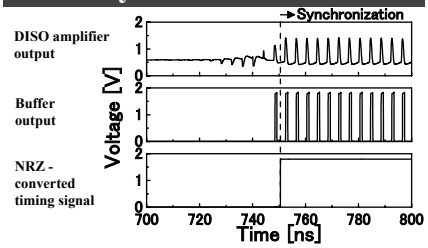
• After amplification and differential / single-ended conversion, inverter buffer performs analog/digital conversion.

Synchronization



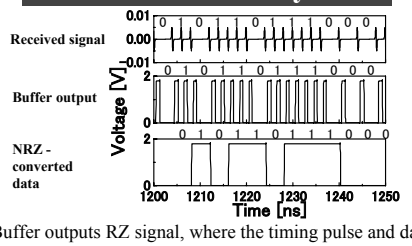
•Transmission rate : 250 Mbps
•Mixer multiplies received signal by template.
• Before synchronization: Delayed clock is unlocked
2nd template is off
•After synchronization: Delayed clock is locked
2nd template is on

Synchronization



•The synchronization establishes around 750 ns.
•NRZ-converted timing signal is used as a flag of the establishment of synchronization, i.e., the signal locks delayed clock.
•NRZ-converted timing signal is also used as a start signal of data acquisition.

Data Recovery



•Buffer outputs RZ signal, where the timing pulse and data pulse is not separated.
•After RZ / NRZ converters, timing pulse and data pulse are separated and converted to NRZ.
•The receiver is succeeding in the recovery of data from alternately coming timing pulse and data pulse. In this simulation, obtained data rate is 250 Mbps.

Summary

•Single-chip UWB receiver with double GMP generators was developed, and synchronization and data recovery of the UWB receiver were investigated using HSPICE simulation.

•Synchronization established between received signal and template signal. The receiver could recover 250 Mbps data from the received signal, which is composed of timing pulse and data pulse.