Wireless interconnect scheme for 3-dimensional stack systems

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Although research and development in 3-dimensional integrated circuit has so far been done, problems such as penetrated via-hole, highly precise chip integration, heat dissipation, and product yield, are not overcome. In order to solve these problems, the 3-dimensional integrated architecture which communicates between multiple chips by wireless interconnect is proposed in our COE program. Two types of wireless connection are studied. One is global connection, which communicates beyond neighboring chips using microwave. The other is local connection, which is pass massively parallel between two chips placed in face-to-face. My main subject is development of the local interconnect scheme using integrated spiral inductor pair. The target is achievement of 100Gbps (1Gbps x 100 channels) wireless communication, without precise tuning for chip positions. The detailed contents of research are as follows.

1. **Design and analysis of baseband transmission code**
    - Devise the transmission code for efficiently centralizing the power spectrum of a baseband signal
    - Study the transmission code which concentrates a power spectrum and simultaneously embeds a spread code
    - Analysis of the above-mentioned code system, and performance evaluation by computer simulation

2. **Electromagnetic-field analysis of spiral inductor pair integrated on chip**
    - Study the multi-port equivalent expression between two or more spiral inductors by electromagnetic-field analysis and network theory

3. **Detailed design and analysis of transmission characteristic of combining the code System and spiral inductor pair**
    - Optimal design for the structure of a spiral inductor pair, a self-resonant frequency, and Q value.
    - Analysis evaluation about the cross talk between connection
    - Examine of the possibility of the dynamic reconstruction using a cross talk

4. **Fabrication and estimation of test chip with spiral inductor pair and transceiver circuit**
    - Measurement and evaluation of resonance frequency and Q value of a spiral inductor pair
    - Measurement and evaluation of a transmitted electric power spectrum

- Measurement of bit error rate and a cross talk

5. Design of communication system which can be reconstructed dynamically between nearby inductor pairs
- Design and evaluation of a reconstruction control algorithm
- Design and fabrication of the transceiver circuit with a dynamic reconstruction function
- Measure the size of a domain which can be reconstructed, and the bit error rate

6. Feed Back the measurement result and the evaluation result to the design model.
- Improvement in reliability of a design method by feed back to the code design and the structure design of spiral inductor pair
- Development of a multi-port equivalent model which can support the system design of dynamic reconstruction scheme

A prototype of the 3-dimensional stack system with five test chips will be designed and fabricated through the above research. The maximum transmission bit-rate, the cross talks and the bit error rate will be measured and evaluated.
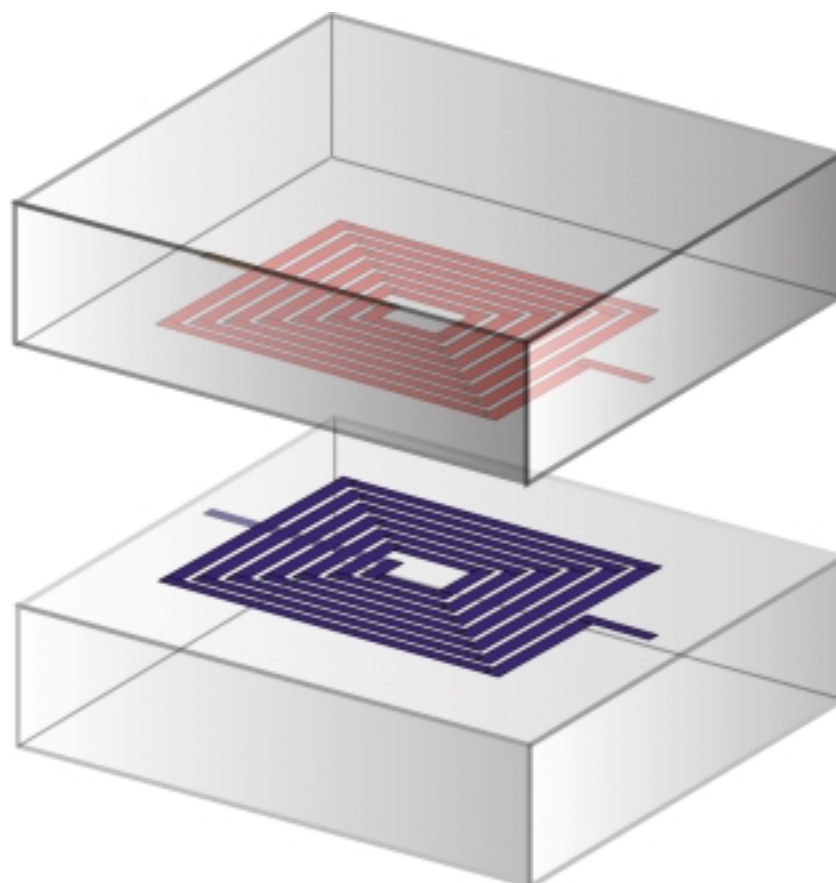

Fig. 1 Spiral inductor pair integrated on the chip realizes wireless interconnect.