Associative-memory-based systems with recognition and learning capability: Research on the required functional memories

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● Towards systems with recognition and learning capability

In order to realize intelligent data processing such as feature extraction, recognition, rough judgment and learning, which are usually done in the human brain, a memory-based, flexible system architecture is proposed. The envisaged system will have distributed processing units, which simultaneously process data stored in a vast likewise distributed memory space, and thus generate the outputs of intelligent processing algorithms. To realize the necessary high-speed, high-capacity interconnects and high-performance input/output (I/O) interfaces across a 3-dimensional integrated-stack system, the COE plans to use wireless as well as optical interconnects in addition to the conventional metal interconnects.

● Functional-memory basis of intelligent systems

The intelligent-system target requires breakthrough solutions for circuits realizing two basic functions: dense, high-interconnectivity data-storage as well as fast, low-power pattern matching. Therefore, we propose area-efficient multi-port memory and fully-parallel mixed analog-digital associative memory architectures. The multi-port memory enables us to push access-bandwidth and interconnectivity beyond the Tb/s and the 30 port level, respectively, while keeping integration area significantly smaller than previously possible. The associative memory provides nearest-match capability between input-data words and the stored knowledge basis of reference-data words. In addition to long input data-words (1-16Kbit) the stored knowledge basis will require a large number of reference-data words (1000-10000 words). In the COE program we aim at integrating the complete matching function in an area-efficient way into the memory, where the knowledge base is stored. Our present concept employs digital processing up to bit-level comparison and fast analog principles for word-level comparison as well as the winner-take-all function. Test-chip designs verify sub-100ns minimum distance-search times at a low power dissipation of

<2mW per reference pattern (Fig. 1). The concept for including a learning function into this associative-memory architecture (Fig. 2) has been developed and has been verified by simulation. The next steps are the hardware verification of the learning function and development of a complete intelligent prototype system including feature extraction of input data, recognition and learning functions as well as a judgment and action-decision unit.

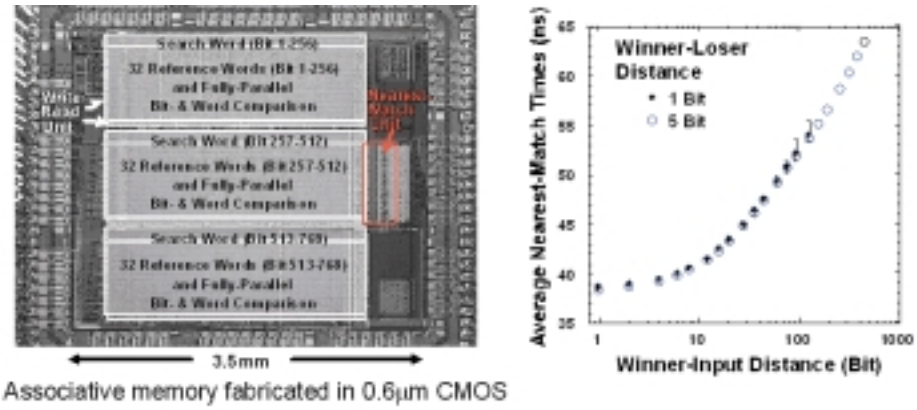

Fig. 1: Fabricated associative memory with 70 ns nearest-match time and 1.35mW power dissipation per reference pattern.

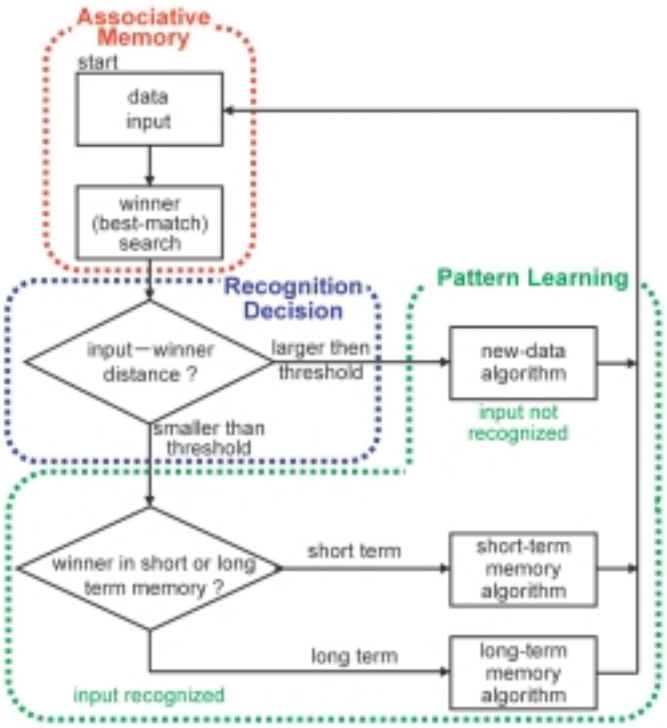

Fig. 2: Learning algorithm based on associative-memory and short/long-term storage.