Image processing front end for associative memory-based systems with recognition and learning capability

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● **Towards realization for an associative memory-based systems with recognition and learning capability**

Pattern recognition and learning are basic functions, which are needed to build artificial systems with capabilities similar to the human brain. The effective implementation in integrated circuits is therefore of great technical importance. The traditional neural network approach emphasizes the role of the processing elements (neurons) and their interconnection network, but neglects sufficient exploitation of the third powerful system-component, which is the memory. Therefore a memory-based flexible system architecture has been studied in order to realize intelligent data processing such as feature extraction, rough judgment, and analogical inference which an usually done in the human brain. In the COE research project, the fundamental study of associative memory-based, flexible system architecture will be carried out by a broad research ranging from algorithm and system to integrated circuit design. Integration methodologies of these results into the 3-dimensional custom stack system (3DCSS) will be also investigated. The aimed-at structure of the associative memory-based systems with recognition and learning capability is depicted in Fig. 1.

This target requires breakthrough solutions for circuits realizing three basic functions: dense, high-interconnectivity data-storage, and fast, low-power pattern matching as well as vision-based intelligent processing. Therefore, we have investigated an area-efficient multi-port memory architecture, a fully-parallel mixed analog-digital associative memory, and a digital real-time image segmentation architecture. The multi-port memory architecture enables us to improve access-bandwidth and interconnectivity, respectively, while keeping integration area significantly smaller than previously possible. The associative memory architecture has been verified to perform pattern-matching in < 100ns with a power dissipation of < 2mW per reference pattern and is extendable to incorporate a learning function. Vision-based intelligent processing requires furthermore extraction of objects from natural images. Our recently proposed and patented digital picture-segmentation architecture is estimated to allow single-chip integration of an object-extraction system from real-time video signals at the 100nm-technology node. In the COE research project, the associative memory-based systems with recognition and learning capability will be realized by combining the research results of these three fields.

● **Image processing front-end : Research on digital real-time moving-picture segmentation and detection**

The vision-based intelligent processing for associative memory-based systems with recognition and learning capability, as shown in Fig. 1, requires segmentation of objects and feature extraction/modeling for data reduction through object encoding. Image segmentation is the extraction process of all objects

from natural input images and is the necessary first step of object-oriented image processing such as object recognition or object tracking. For such image segmentation and feature extraction, we are developing new methodologies suitable for associative memory-based systems. Fig. 2 (a) shows a conceptual example of an image segmentation and feature extraction systems.

A farther aim of our project in the COE program is to develop high-speed and high-density image segmentation algorithms and chip architectures, applicable to real-time moving pictures and thus enabling vision-based intelligent processing. We have proposed a highly-parallel digital algorithm for gray-scale/color image segmentation of real-time video-pictures and a cell-network based digital VLSI implementation architecture. A small-size test chip has already been fabricated and functions correctly (Fig. 2 (b)). The next development steps are the verification of our proposed architecture for large-sized images by a large-size test-chip design and an extension of algorithm and architecture to the application of moving-object detection.

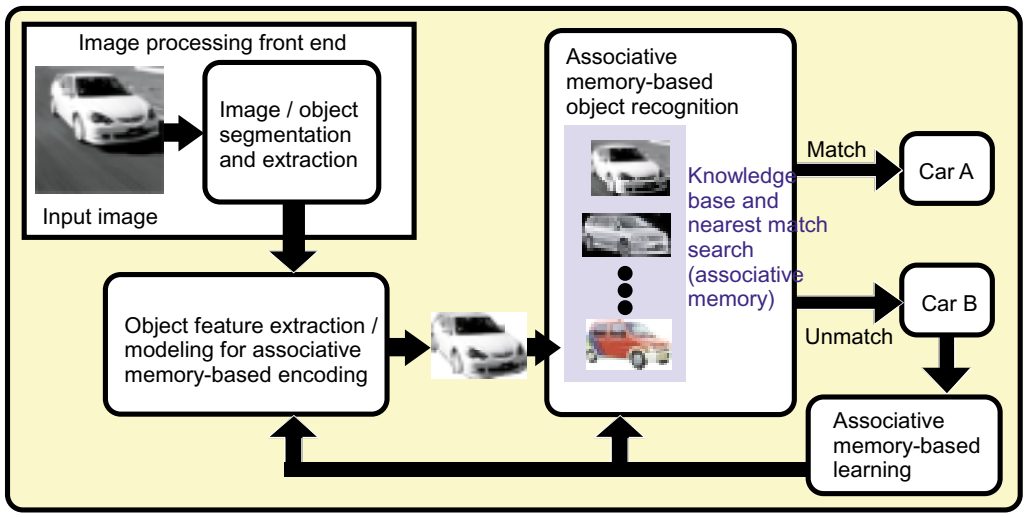
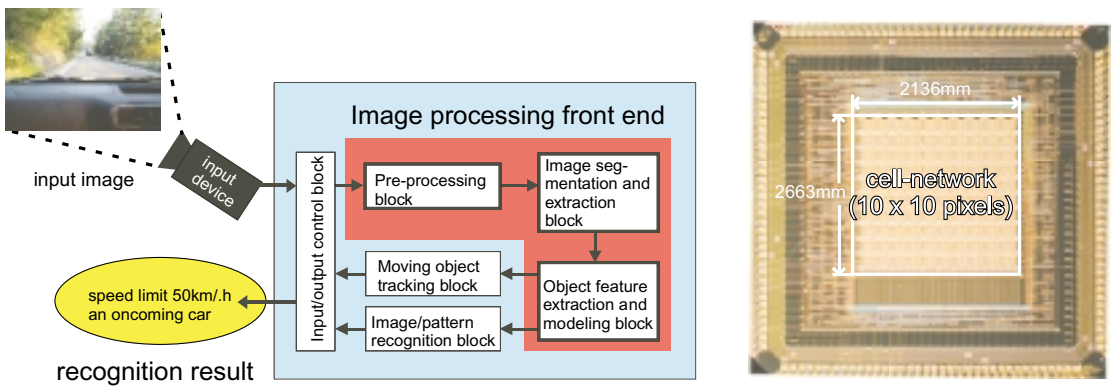


Fig. 1: Structure of envisaged associative memory-based systems with recognition and learning capability.



(a) A block diagram of image segmentation and feature extraction for real-time applications

(b) Image Segmentation Test-Chip (0.35μm CMOS Technology)

Fig. 2: Image segmentation and feature extraction system for real-time applications.