Research of 3D SOI Transistors

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● Research Background

The trend of packing density and performance innovation in large-scale integration (LSI) has started in 1970 resulting in one-million fold increases in memory magnitude and processor performance 30 years after. This has been achieved mainly by patterning techniques in the former 15 years and structure evolution in the latter 15 years, as shown in Fig. 1.

Along with the trend, transistors consisting of the LSI has been scaled down to 1/100 these 30 years achieving 100-fold switching speed and 1/10000-fold power consumption in principle. The characteristics that finer patterning derives higher performance have been driving the LSI trend. As a result, the evolution of machine civilization with present information technologies has been driven by the LSI trend.

● Role in COE project

Along with the scaling, fine transistors have become close to operational limits caused mainly by the short-channel effect. Then, the development of three-dimensional (3D) transistor structures has been accelerated as 3D structures of memories which had been already developed. The author presented some ideas that side-walls of a trench formed into silicon substrate were used as transistor channel when he invented a trench memory cell of DRAM, as shown in Fig. 2. This concept of from 2D to 3D may be a general trend in various fields.

The transistor as a key component of LSI should be fabricated with minimum cost. Therefore, conventional planar transistor may continue to be a main component however, clarification of performance and limits of 3D transistor is still very important to revolutionize the LSI.

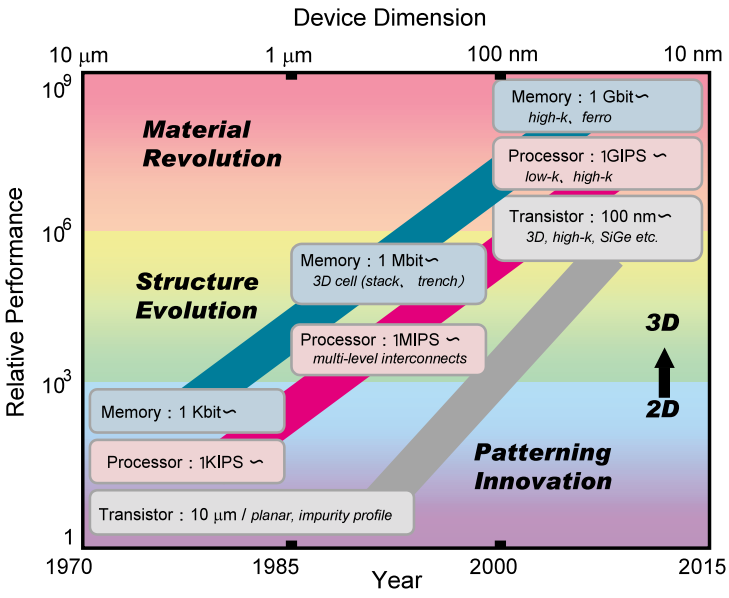

Fig. 1 Technology progress in large-scale integration (LSI).

Research Items

The author's group achieved a beam-channel 3D transistor of 2-μm channel length with a beam of 1 μm in height and 54 nm in width in 2001 and that of 0.2-μm channel length with a beam of 500 nm in height and 40 nm in width in 2002. They are operated successfully. If these 3D transistors might be incorporated in actual LSI's, they should be CMOS at less than 50-nm channel length node. Thus, SOI 3D transistors are planned to be developed.

Research and development items to realize these transistors are as follows;
* ultra-narrow beam delineation, * vertical gate formation, * self-aligning with gate and source/drain, * low-resistive source/drain, and * low contact resistance.

Furthermore, to obtain adequate transistor performance, means such as:
* short-channel effect suppression and * threshold voltage control.

Summary

Leading-edge research has revealed that the ultimate transistor dimension might be around 10 nm. Thus, this is expected to be given birth to 15 years after if the present scaling trend continues at the same rate. However, the practical use of 3D structures strongly depends on future R&D. Our group would like to contribute to the R&D.

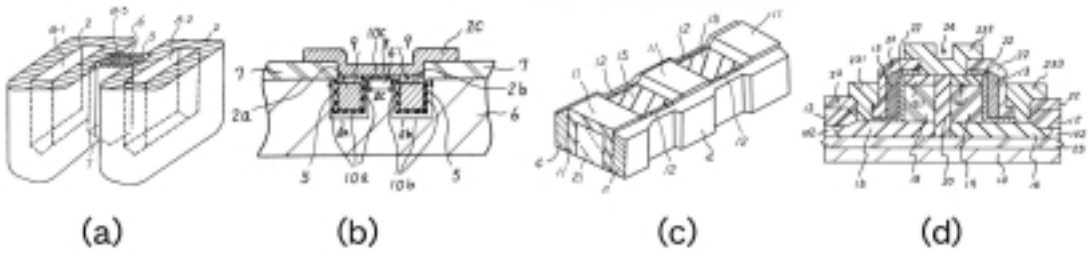

Fig. 2 Patent applications by the author such as (a) side-wall channel in silicon substrate trench (applied in 1975, JP#13443866), (b) multi-channels including side and upper walls (applied in 1983, abandoned), (c) side-wall channel transistor and memory (applied 1983, USP#4937641), and (d) side-wall SOI CMOS transistor (applied in 1983, USP#4670768).

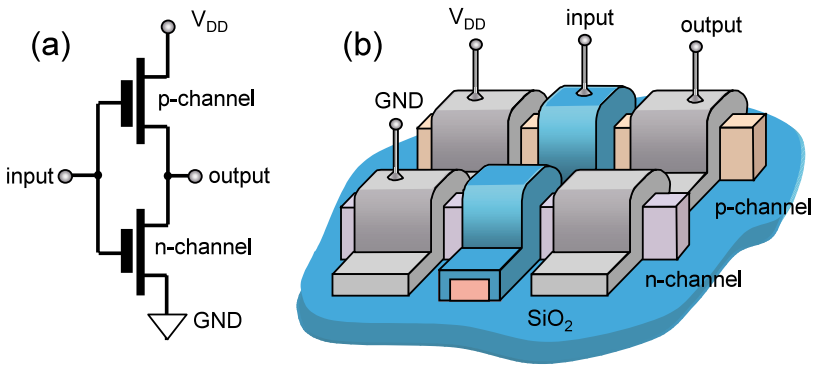

Fig. 3 Fundamental CMOS gate (a) and the corresponding beam-channel CMOS transistor, (b) formed on silicon-on-insulator (SOI).