Nanodevices and Systems
Fundamental device scaling techniques

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● Fundamental device scaling techniques in our COE program

The research center for nanodevices and systems, Hiroshima University is the core of our COE program and is well known having a world leading level clean room and sub-100-nm device fabrication facilities. The aim of the sub-subject named "Fundamental device scaling techniques" is achieving innovative research outputs concerning process and device technologies that will bring further evolution in scaled device performance and function. Development of new generation devices depending on mainly the bulk-planar scaling rule will be more difficult in near future. Improvement in device performance will continue introducing new technologies to their structure and fabrication process gradually. I am mainly working on research of FEOL (Front End of Line) that is the first half of integrated circuit fabrication, in other words, a core part of FET fabrication.

One of our aim through the COE program is education of young people who have wide technology background. In future, engineers working in a integrated circuit field will be required changing their viewpoints freely from device side to circuit side to flexibly cope with interdisciplinary problems. A practical education platform set in our COE program is development of 3DCSS system utilizing optical or wireless interconnects. In the case of "Fundamental device scaling techniques", one approach for this education purpose is collaboration with modeling or circuit design groups to demonstrate effectiveness of newly developed technology based on device level achievements. In addition to such a direct approach, for the young people in our COE team, learning the technical essence from additional technical fields with high research level through the program will be very valuable.

Hereafter, my research activities are described.

● Ultra-shallow Junction Formation

Source and drain that are an entrance and an exit of main current flow in MOSFETs have been modified shallower and shallower as the MOSFET scaling progressed. Nowadays, the junction depth must be shallower than 20 nm for leading edge devices. Introduction of dopants into Si mainly depends on ion implantation method. For dopant activation after the implantation, a short duration annealing of several seconds order, that is, RTA(Rapid Thermal Annealing) is mainly used in a manufacturing field to minimize dopant diffusion during the annealing. We have succeeded 10 nm junction formation using a new annealing method that replaces RTA. In Fig.1, B depth profiles for junctions with a depth of 9.5 nm fabricated with KrF excimer laser annealing are shown. Diffusion during annealing was smaller than 0.2

nm by utilizing short duration pulse laser with FWHM of 38 ns. We have found that sheet resistance can be reduced less than 1 kΩ/sq. by heating a substrate to 450℃. This means dopants are activated with high efficiency even with such a short duration annealing method. We plan to find and solve the problems that will emerge by applying the laser annealing to device fabrication. Proposed post-RTA techniques, including the laser annealing, have advantages and disadvantages against RTA. We will continue the investigation to find suitable device structures and materials to each developing new annealing methods.

● Workfunction tuning technology for metal gate MOS

Recently, MOSFET performance improvement has been accelerated by thinning the gate insulator aggressively. However, poly-Si that is popularly used for gate electrodes has a depletion problem that leads to saturation in effective insulator thickness thinning. Although metal gates have been investigated to avoid this problem, metal workfunction tuning in order to fit it to the adequate values for both pMOS and nMOS is still remained as a problem. Recently, workfunction tuning utilizing pileup formation at the metal/insulator interface has been reported and research activities of this subject was enhanced. We found that Mo workfunction shift of -0.4 eV was achievable by nitrogen solid-phase diffusion from a TiN film deposited on Mo. The magnitude of the workfunction shift can be modified by changing the pileup nitrogen concentration. Figure 2 shows nitrogen depth profile in Mo MOS structures. In the case of the nitrogen solid phase diffusion, the pileup formed at the Mo/SiO_2 interface is clearly seen in this figure. Deep Nitrogen implantation through the Mo film into Si substrates lead to larger workfunction shift, however, this simultaneously gave rise to unfavorable oxide damage. To improve this method for the manufacturable level, magnitude of the workfunction shift must be enlarged to about -1.0 eV without degrading insulator and interface characteristics. We will continue this work collaborating with other COE members utilizing their knowledge and techniques concerning materials, characterization, and devices.

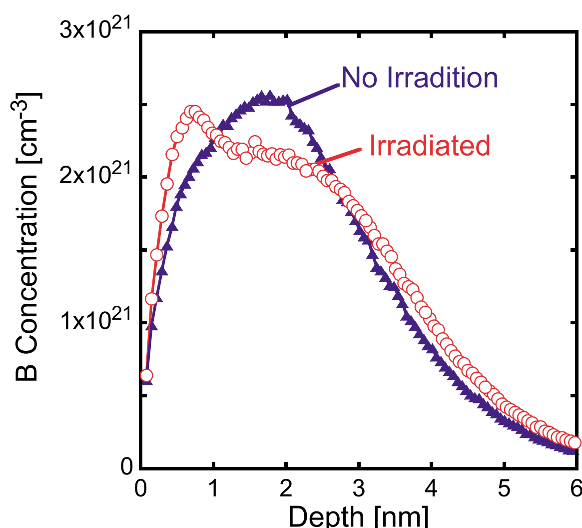

Fig. 1
B depth profiles, obtained with Secondary Ion Mass Spectrometry (SIMS) technique, in ultra-shallow junctions with a depth of 9.5 nm formed with KrF excimer laser annealing. Diffusion caused by the laser irradiation is smaller than 0.2 nm.

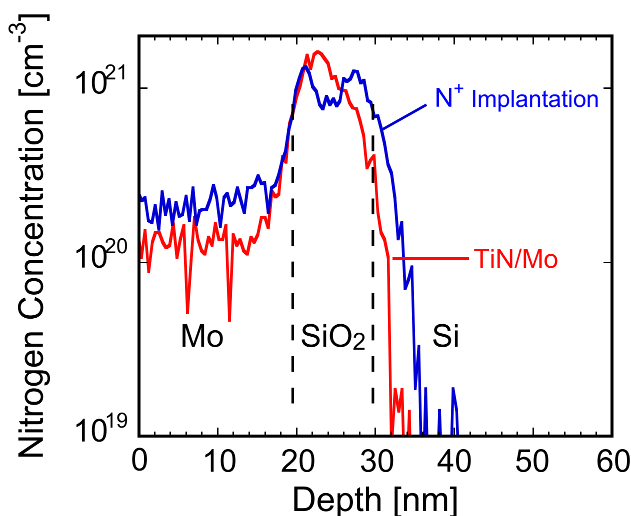

Fig. 2
Nitrogen depth profiles in Mo MOS structures obtained with a back-side SIMS technique. For the specimen doped by solid phase diffusion with a TiN film, nitrogen piled up at the upper interface, namely at the Mo/SiO_2 interface. On the other hand, for the specimen that nitrogen was implanted, nitrogen pileup is observed for both upper and lower interfaces of SiO_2. Thus, impurity pileup formation at the upper interface is the key to shift metal workfunction without causing damage problems.