Low resistive gate electorde/high-k gate dielectrics stacked structure and its device application

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The primary device used to build Large scale integrated circuits(LSI) is the MOS transistor(MOSFET). The device performance is improved by a systematic reduction in size called "scaling". As MOS transistors are scaled deep into the sub-100nm, the gate oxide thickness of these devices is shrinking as well. Since the gate insulator of future devices may not be pure SiO_2, one can define an equivalent oxide thickness (EOT) for a material or a stack of materials as the thickness of pure SiO_2. The International Technology Roadmap for Semiconductors (ITRS) suggests that the EOT must decrease from about 2.0 nm in 2001 to well below 1.0 nm in the next 5 to 7 years. Doing this is extremely challenging because the leakage current through this gate oxide increases sharply with decreasing thickness. Many groups are investigating solutions to this problem. Typically this involves using gate insulator materials with a much higher permittivity(high-k) than SiO_2. The search is spurred by the urgency to rein in power consumption, particularly for battery-driven high-performance devices such as advanced memories. Also, for implementing advanced MOSFET with the high-k material ,the new electrode material with low resistivity is required. So far, however, promising high-k materials and low resistivity gate material also bring electrical disadvantages and processing difficulties.

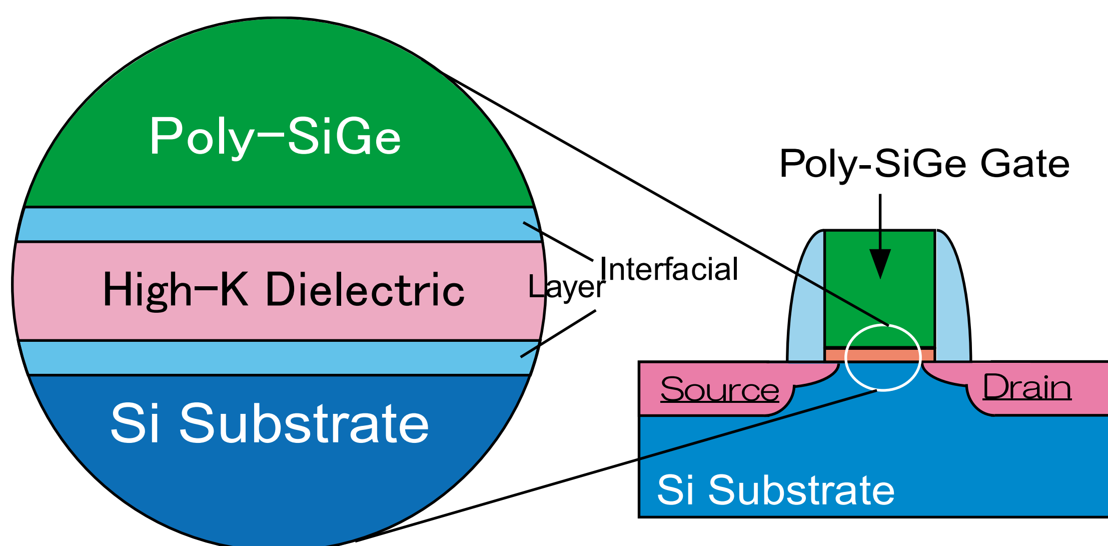
Polysilicon gate depletion can arise when the polysilicon is not doped heavily enough. That problem will be more serious in the case that the EOT of gate dielectric is thin. This problem is a concern especially when the concentration of the channel region approaches that of the polysilicon gate. Gate depletion results in an additional capacitance in series with the gate oxide capacitance. This will reduce the overall gate capacitance and therefore degrade the performance of the transistor.

The new gate dielectric material is essential to implement the high performance MOS transistor for next generation LSI. Therefore, We are investigating the new gate dielectric material, gate electrode material and their matching.

We focus on the poly Silicon Germanium(poly-SiGe) gate as the replacement for conventional poly silicon gate. A poly-SiGe gate electrode minimizes the gate depletion effect, therefore, a high level of dopant activation in the gate electrode is realized even in the low-temperature thermal process. Therefore, poly-SiGe is one of the promising candidate.

The chronology of our efforts are as follows:

1. Investigating the gate new material from the view point of a reactivity with high-k dielectrics and controlability of workfunction.
2. The suppression of the reaction(or atomic diffusion) on electrode/gate dielectric interface.
3. Measuring the defect state density in gate electrode/gate dielectric interface. From that result, finding the conduction mechanism of the gate leakage.
4. By using the technology identified above, we fabricate the 30-100nm gate length MISFET with high-k gate dielectric and a new gate electrode.



Cross-sectional view of MOS transister and gate electrode(Poly-SiGe)/high-k stacked structure. An interfacial layer was formed at high-k/electrode and high-k Si substrate interface. Therefore, expected perfomance improvement cannot be obtained. It's need to supress the growth of interfacial layer.